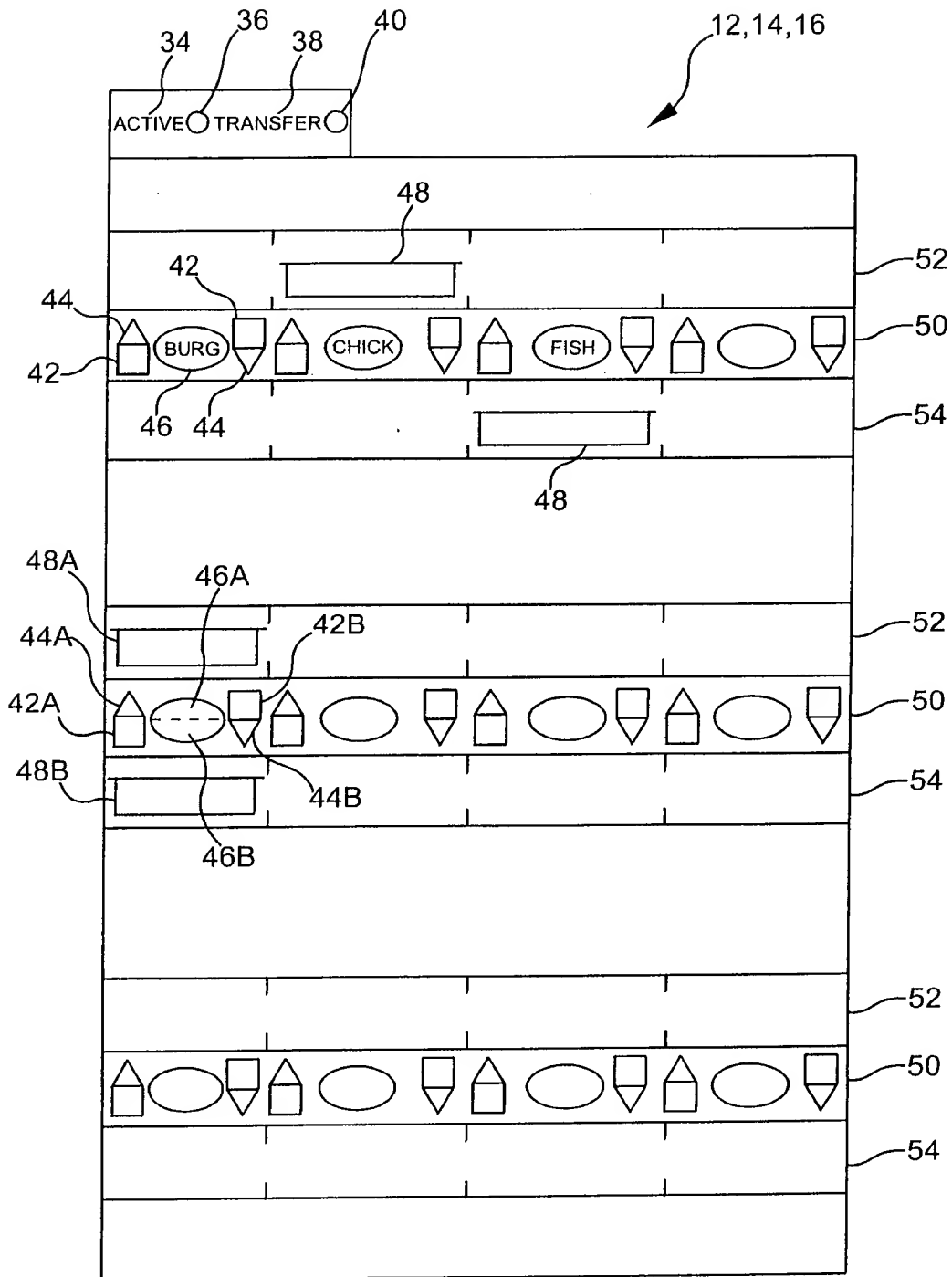
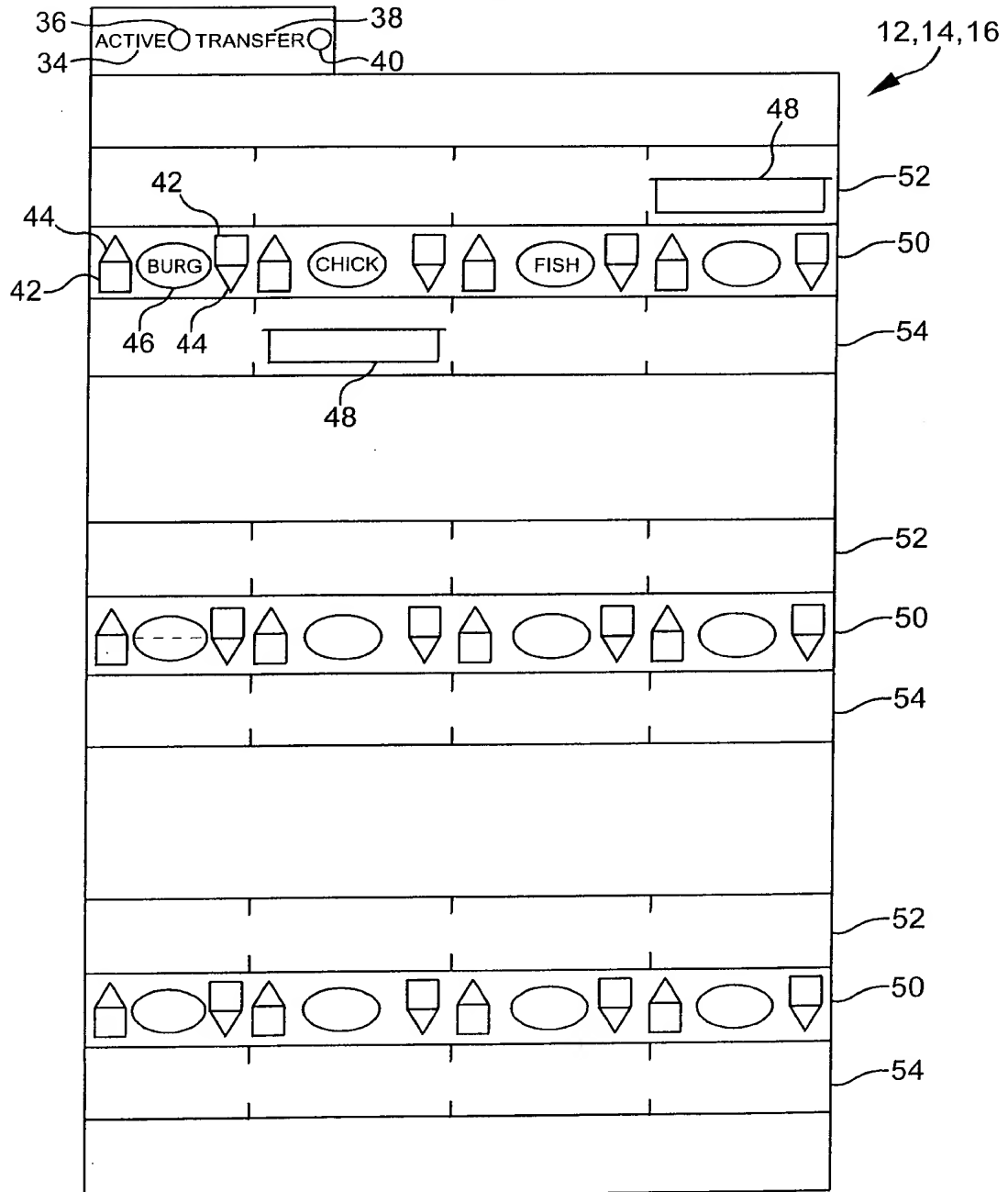


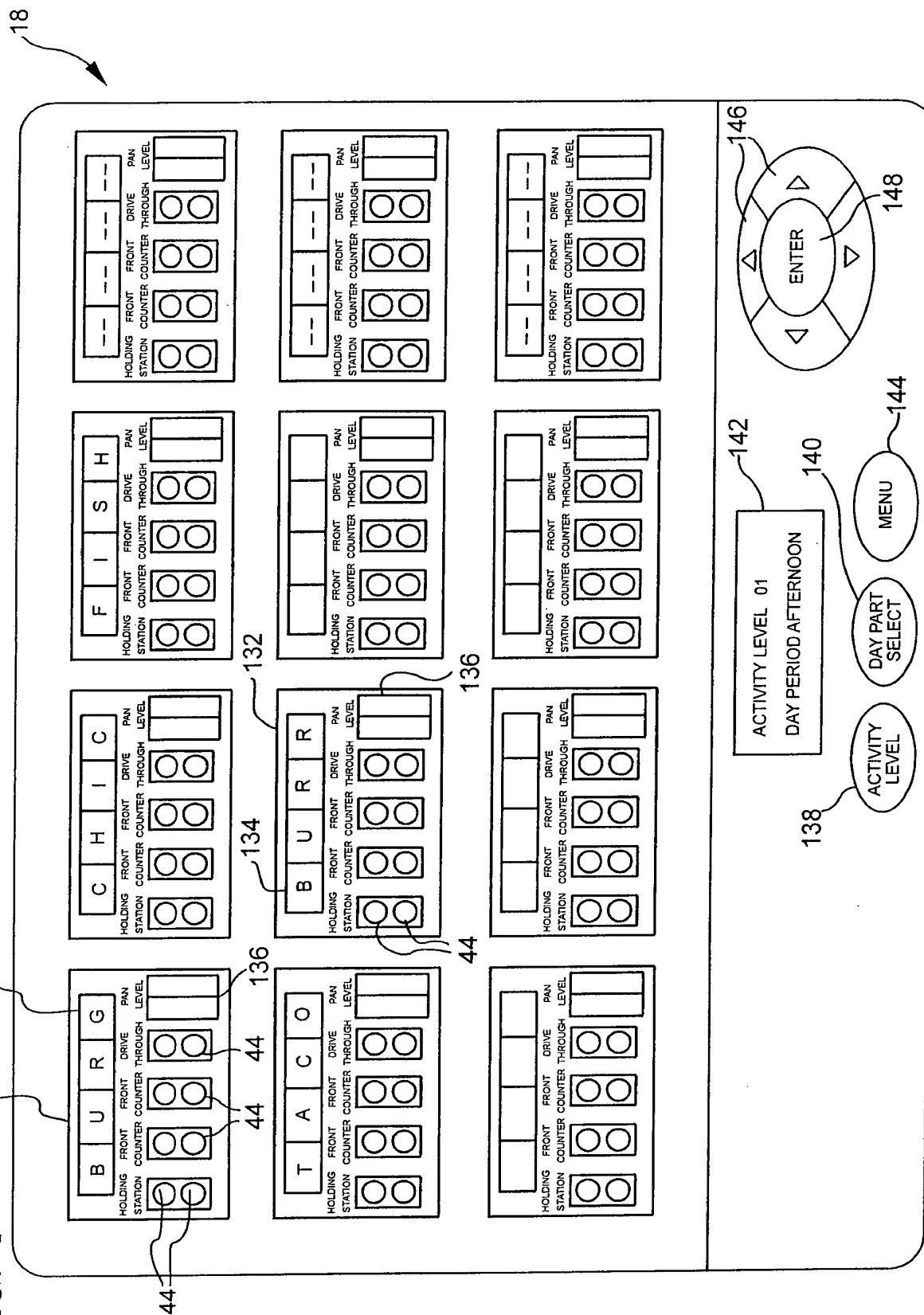
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FIG. 2





132 134



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FIG. 5A

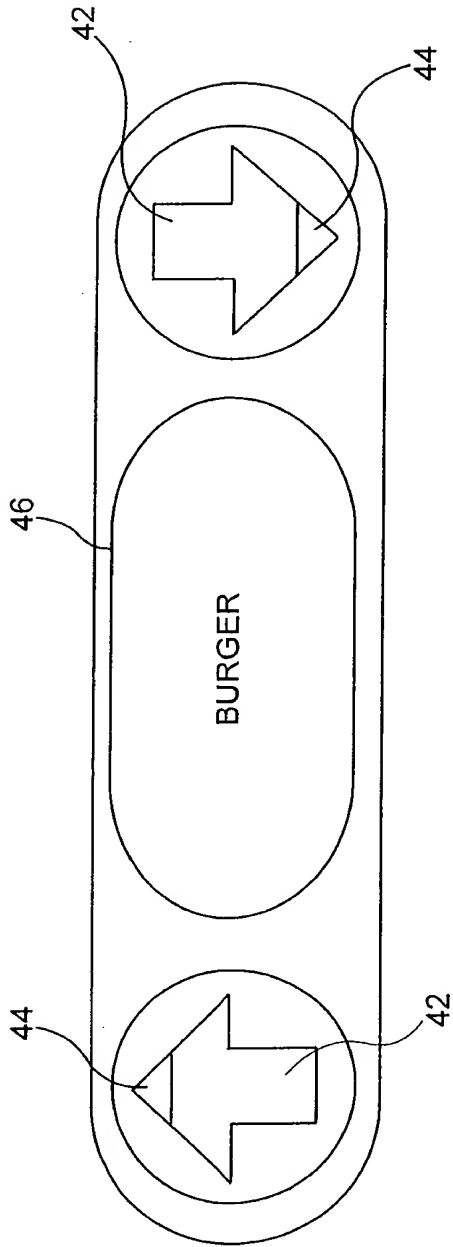
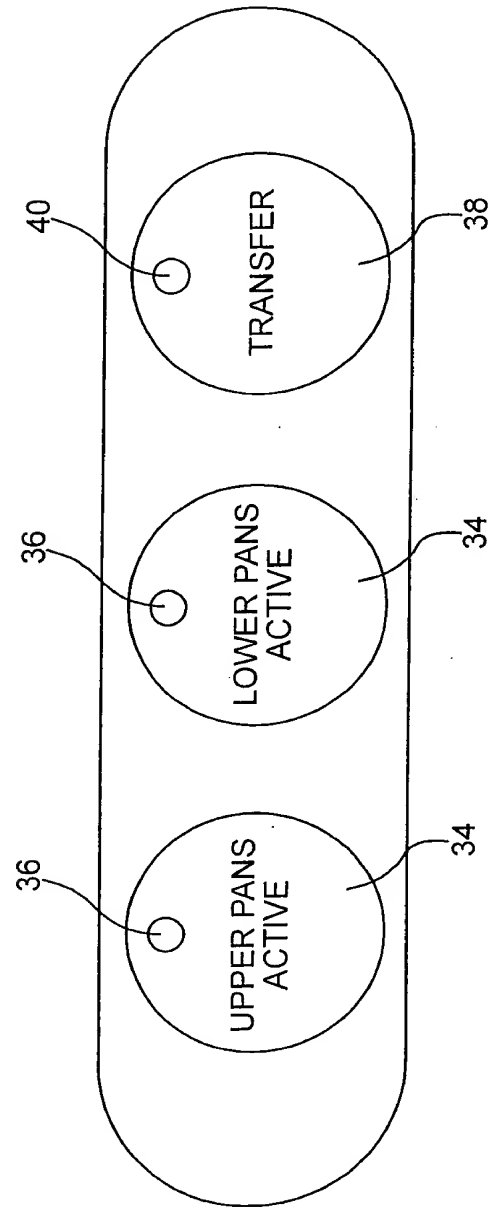
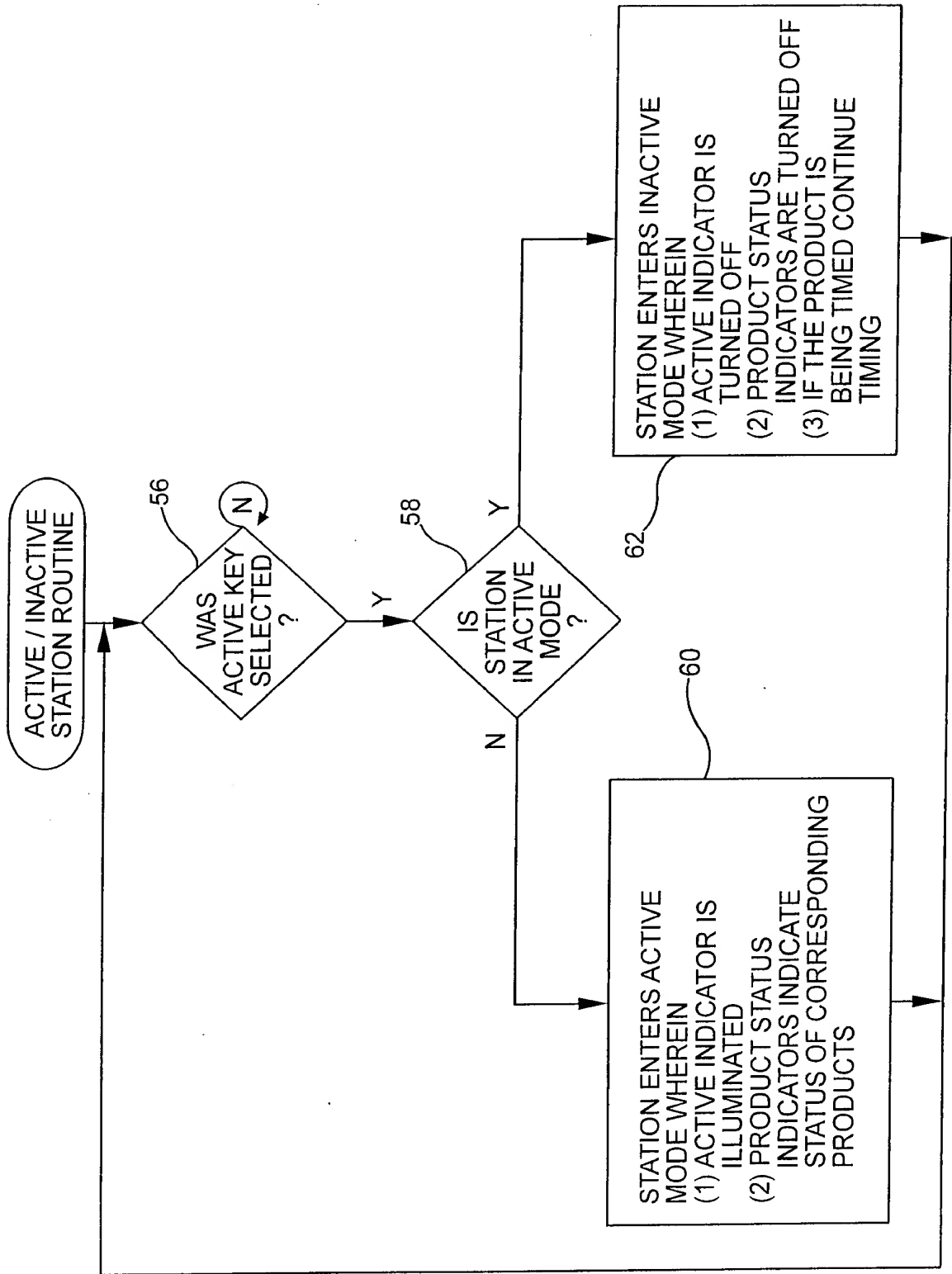


FIG. 5B



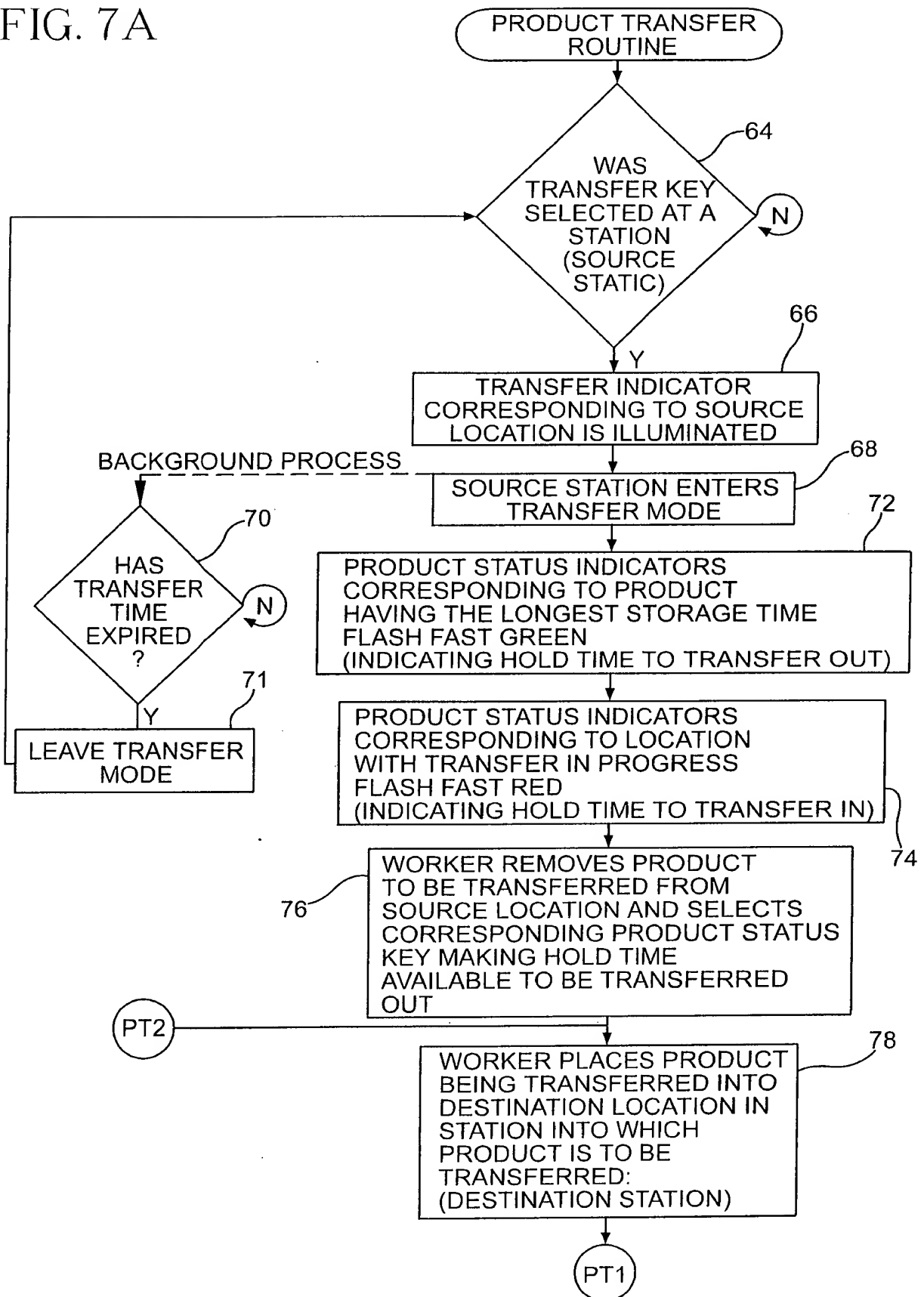
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FIG. 6



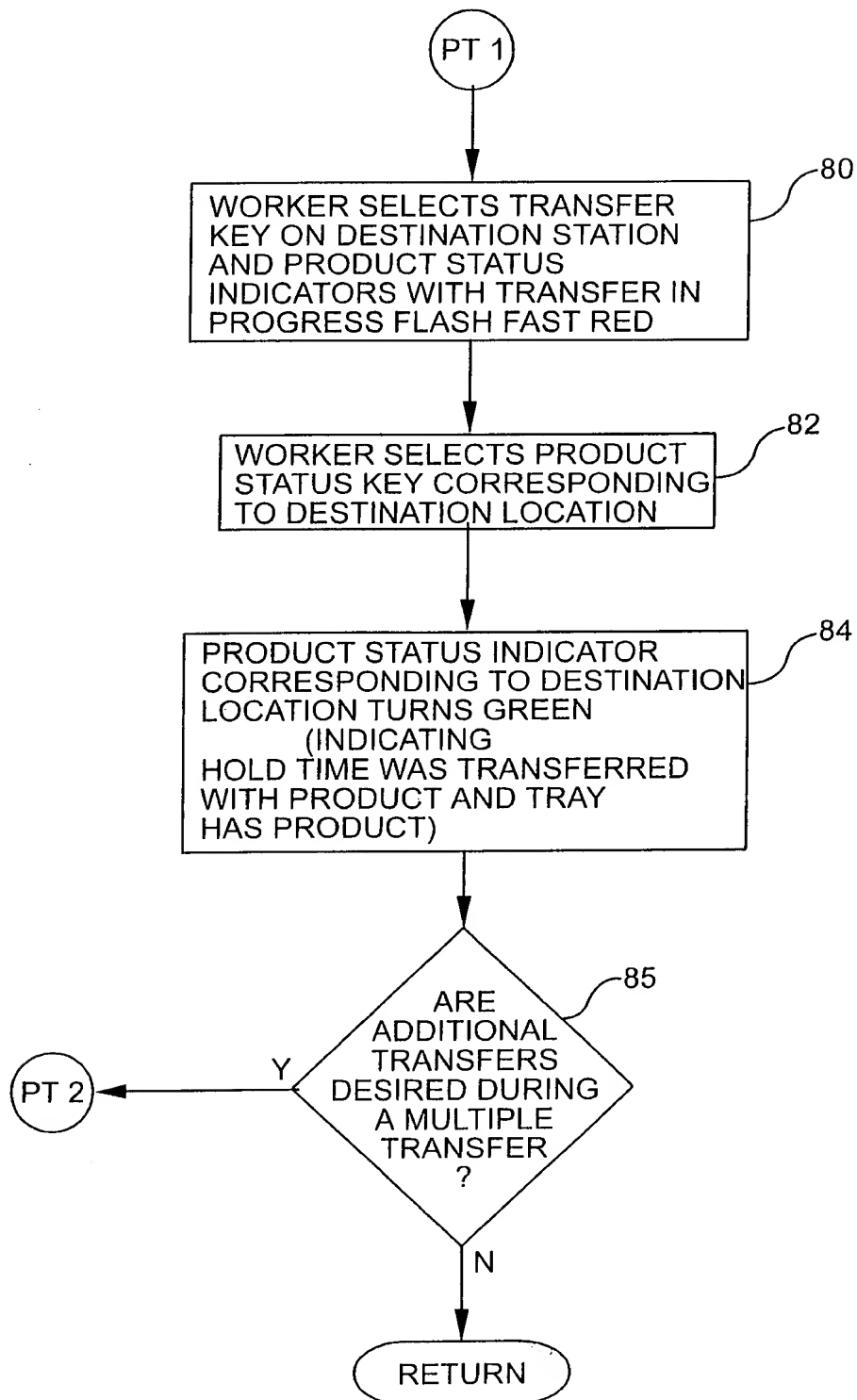
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FIG. 7A



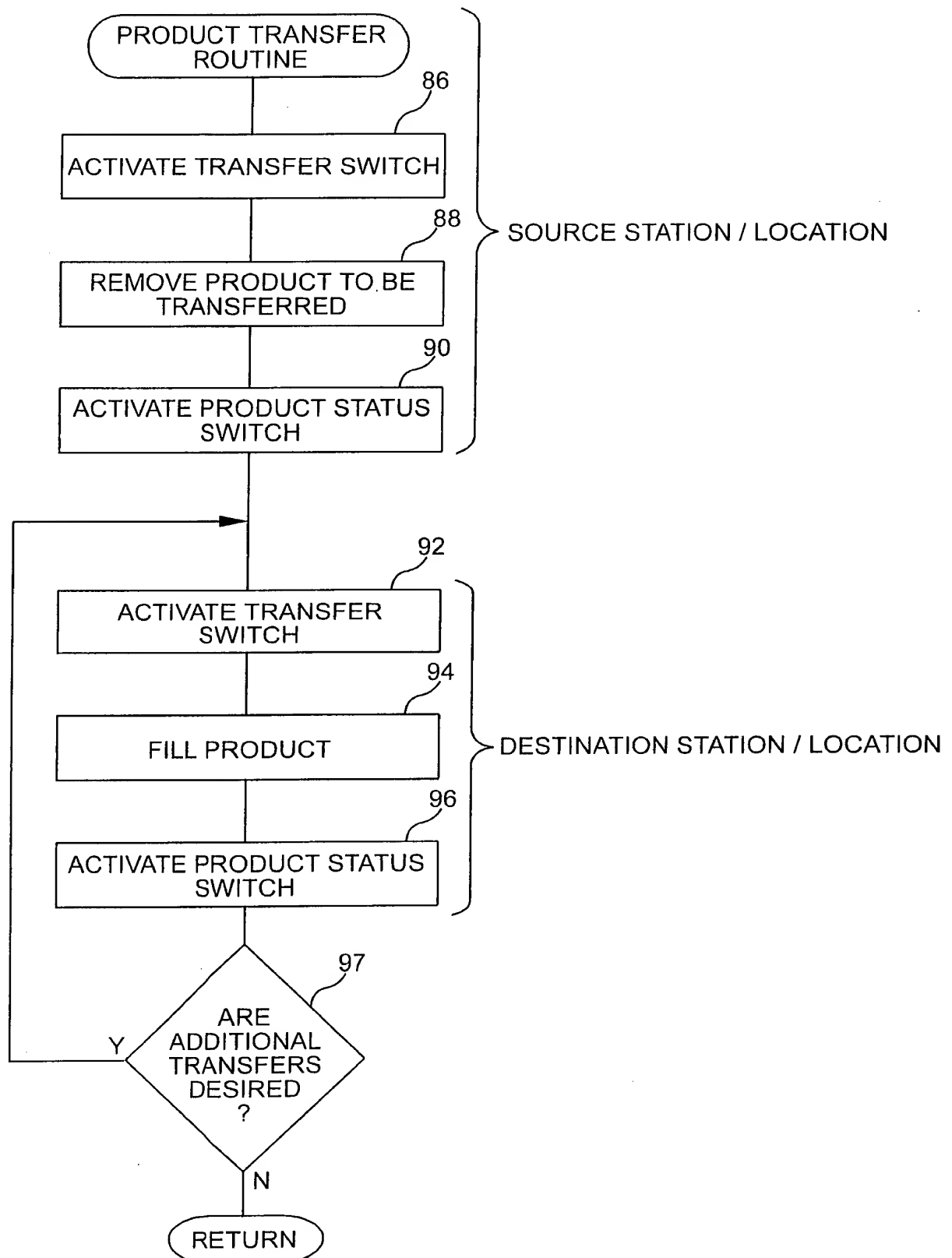
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FIG. 7B



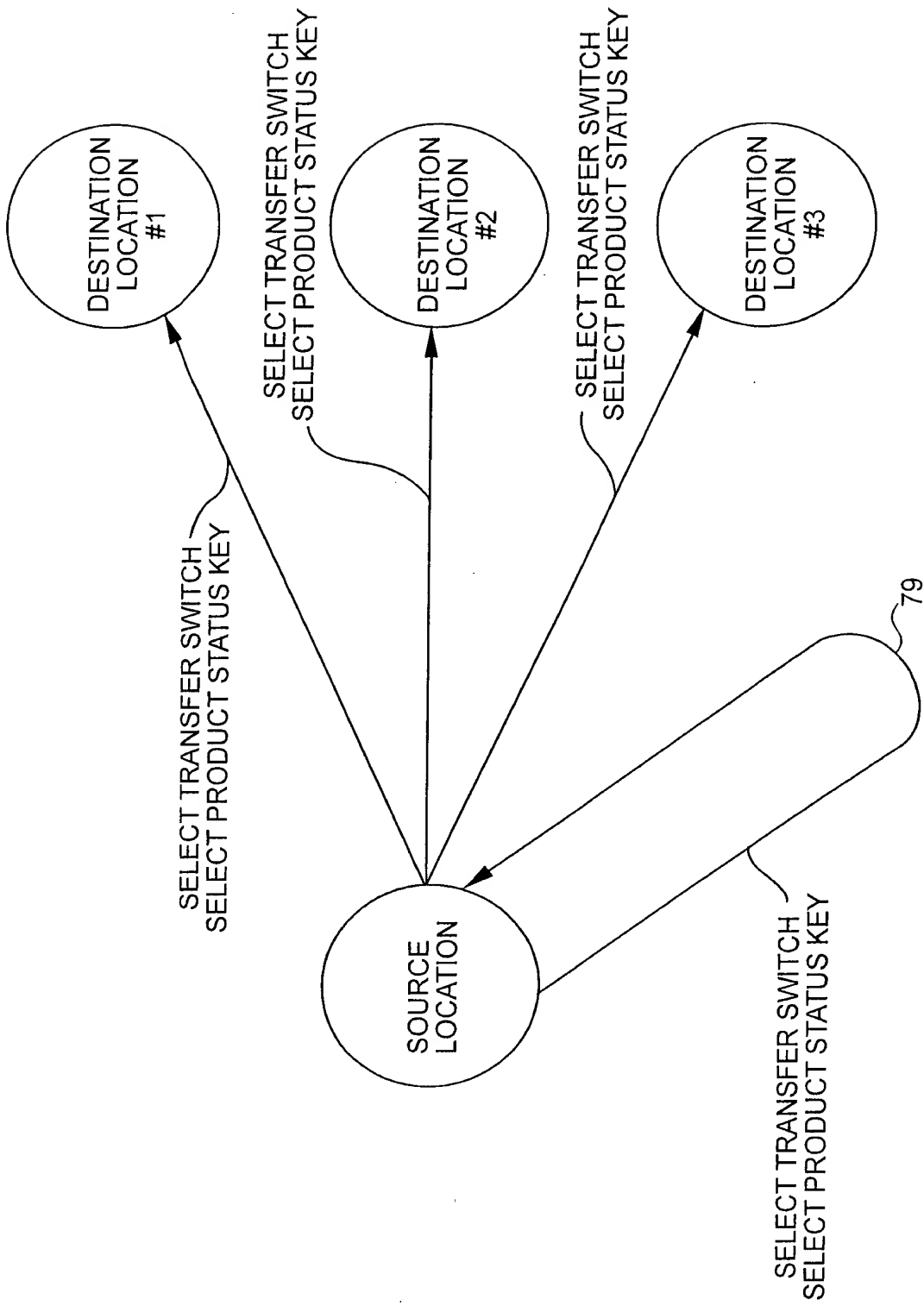
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FIG. 8A



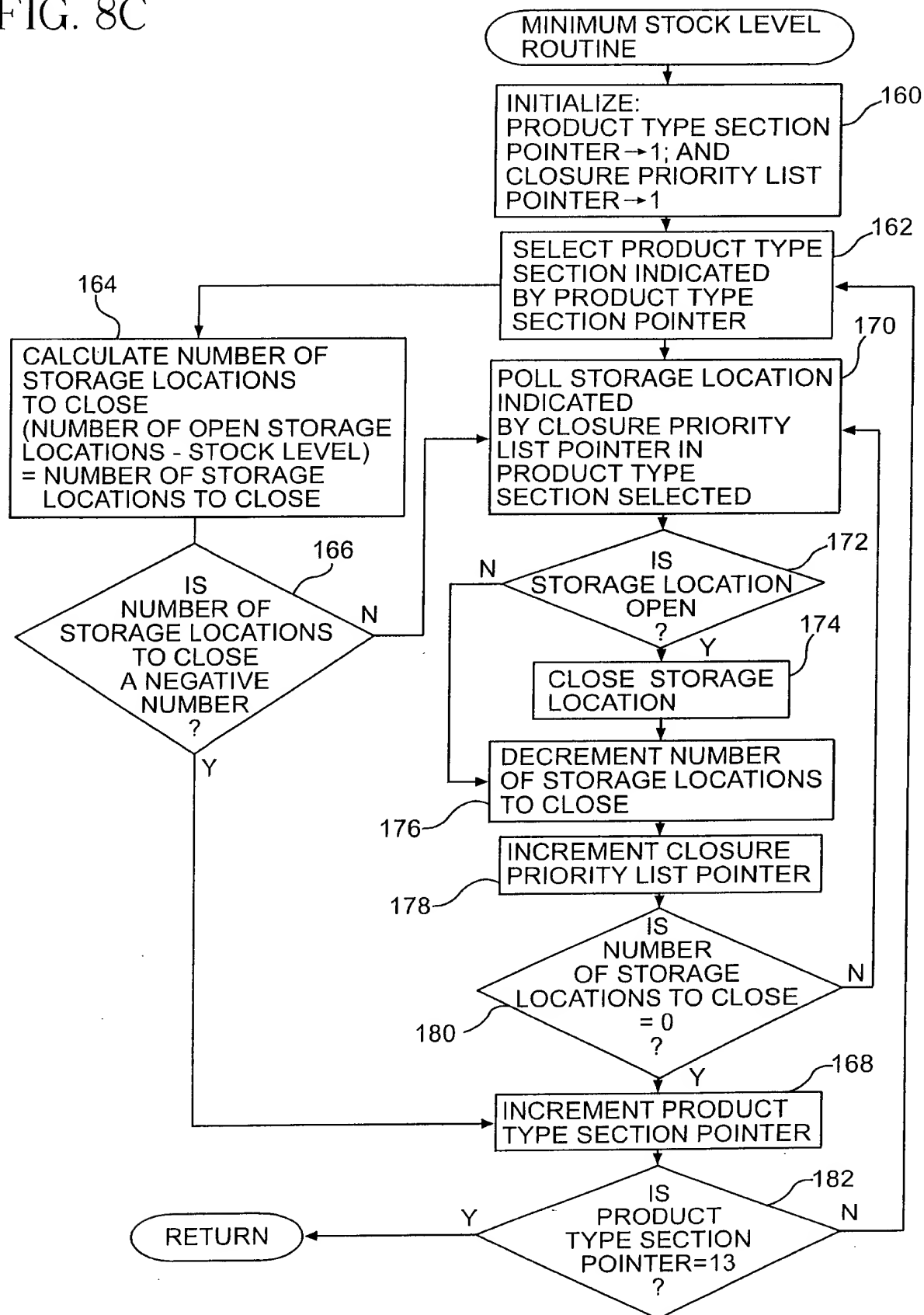
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FIG. 8B



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FIG. 8C



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FIG. 8D

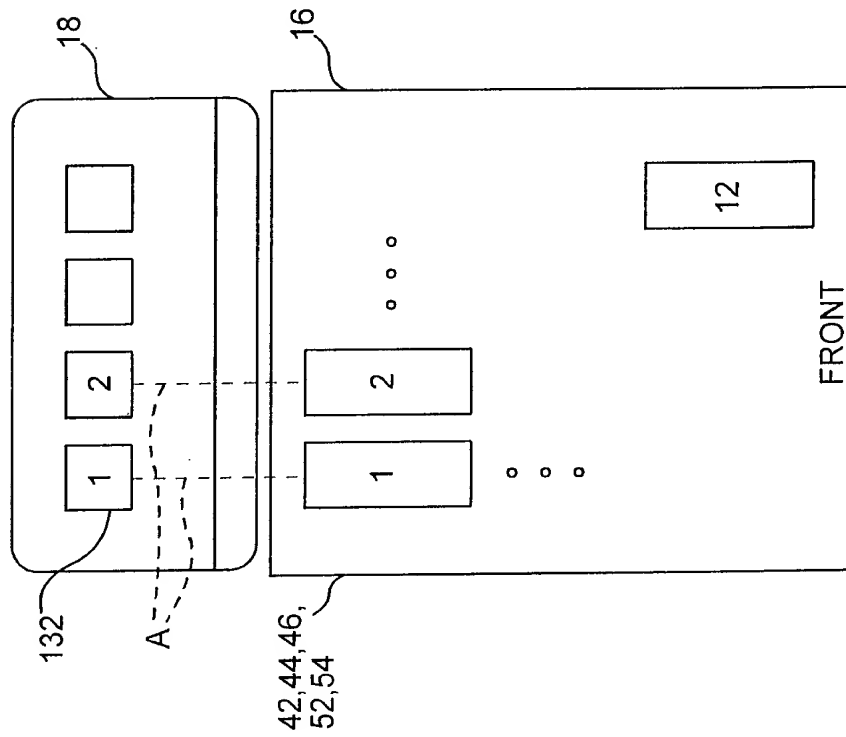
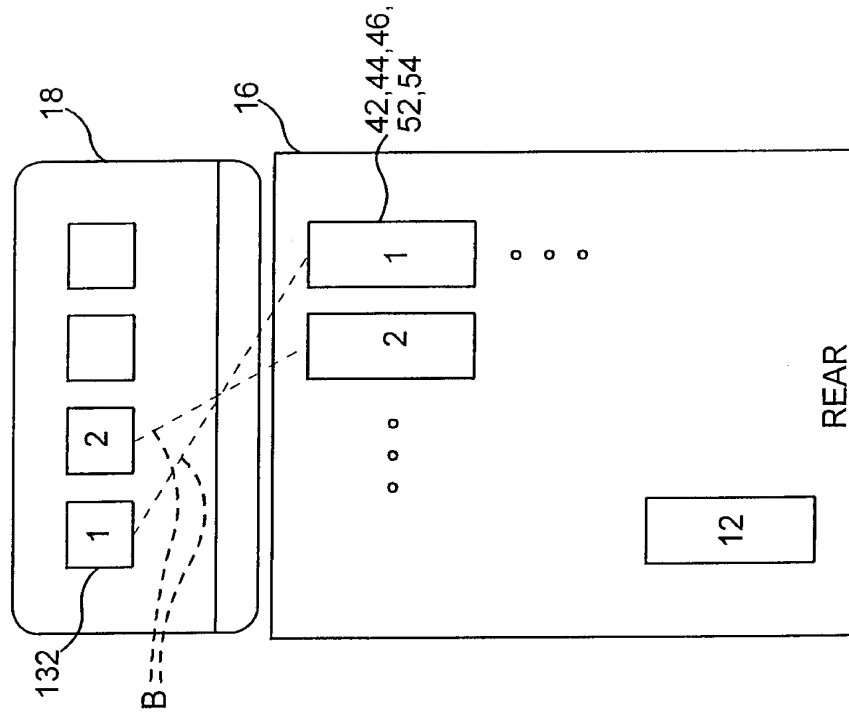
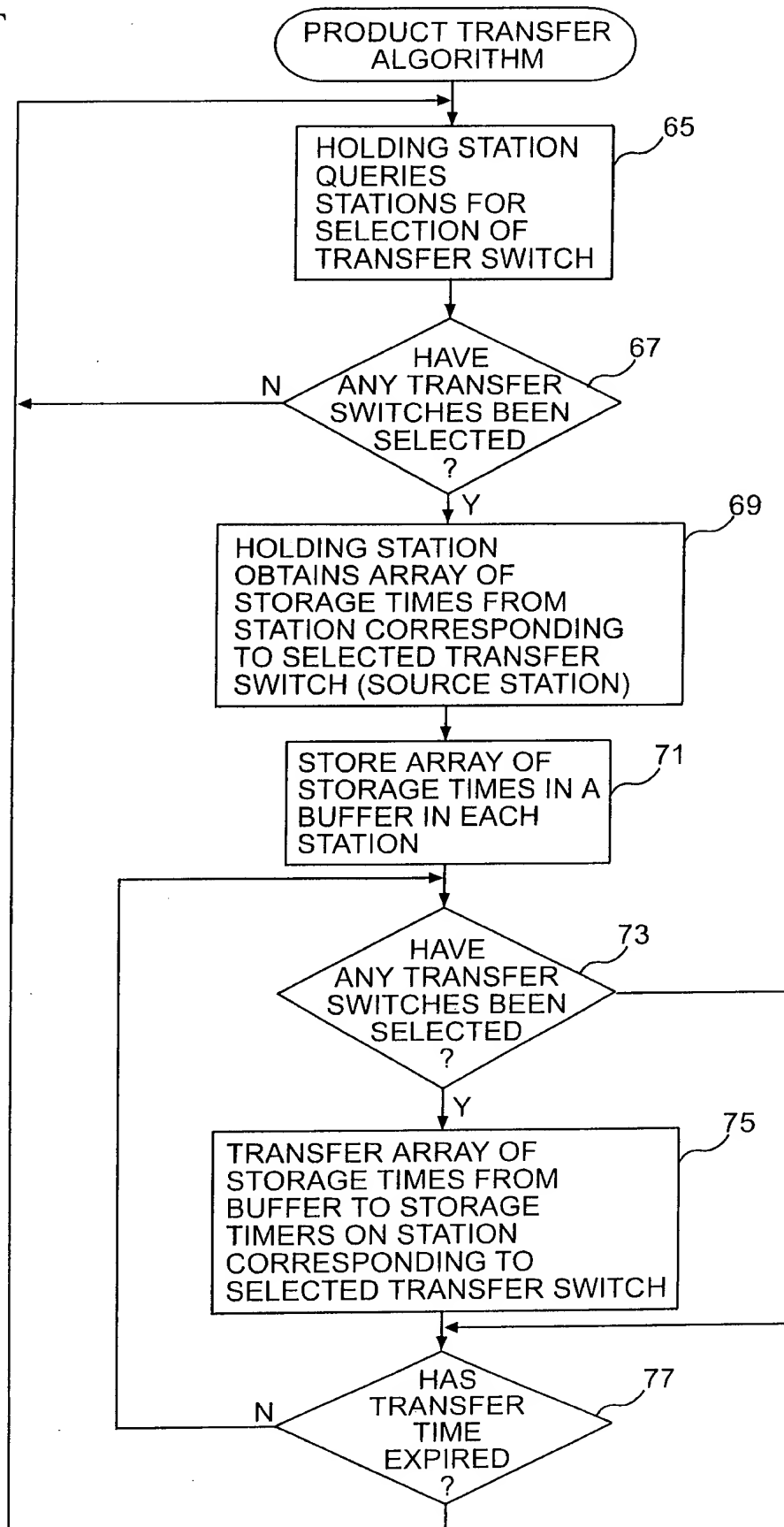


FIG. 8E



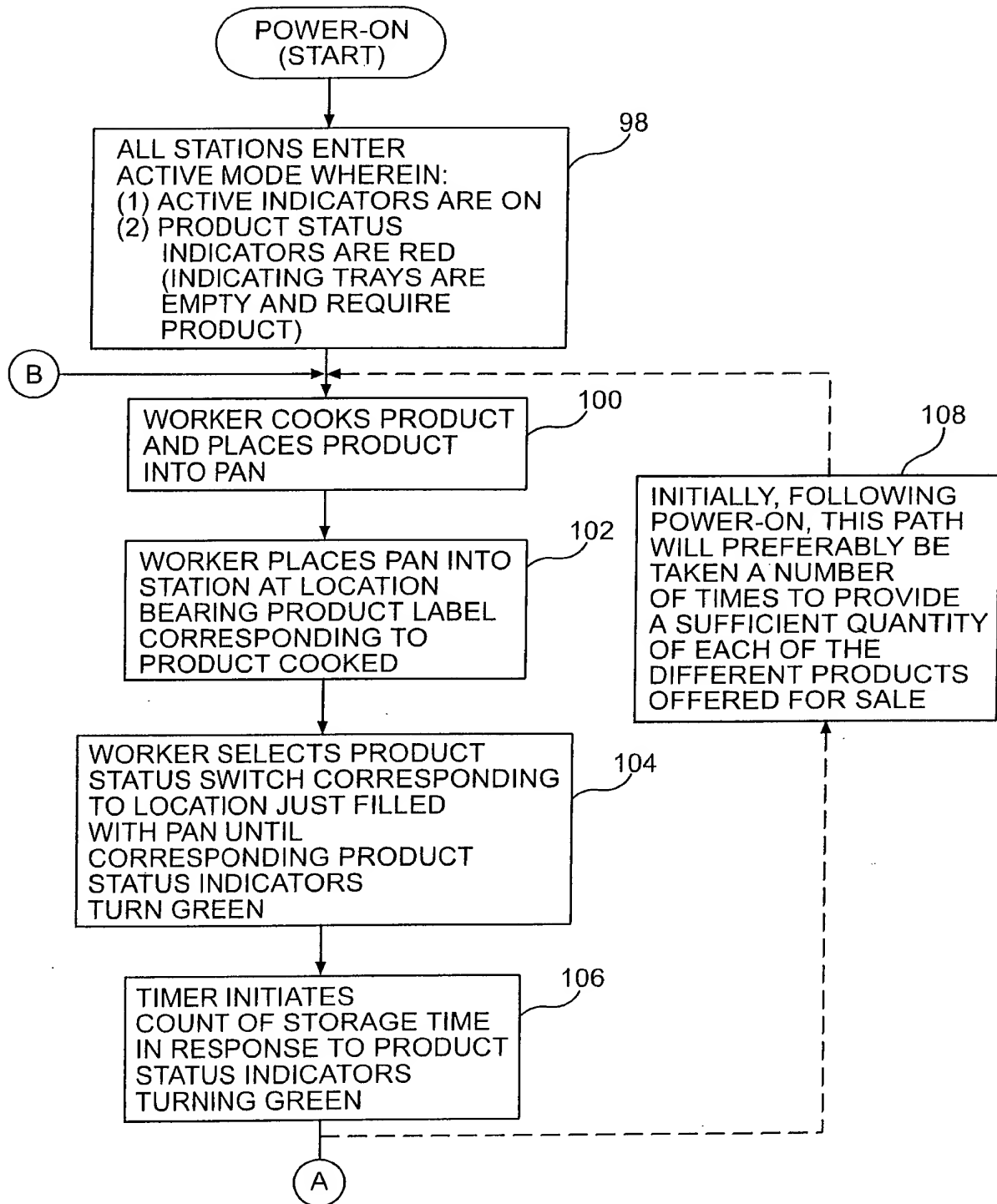
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FIG. 8F



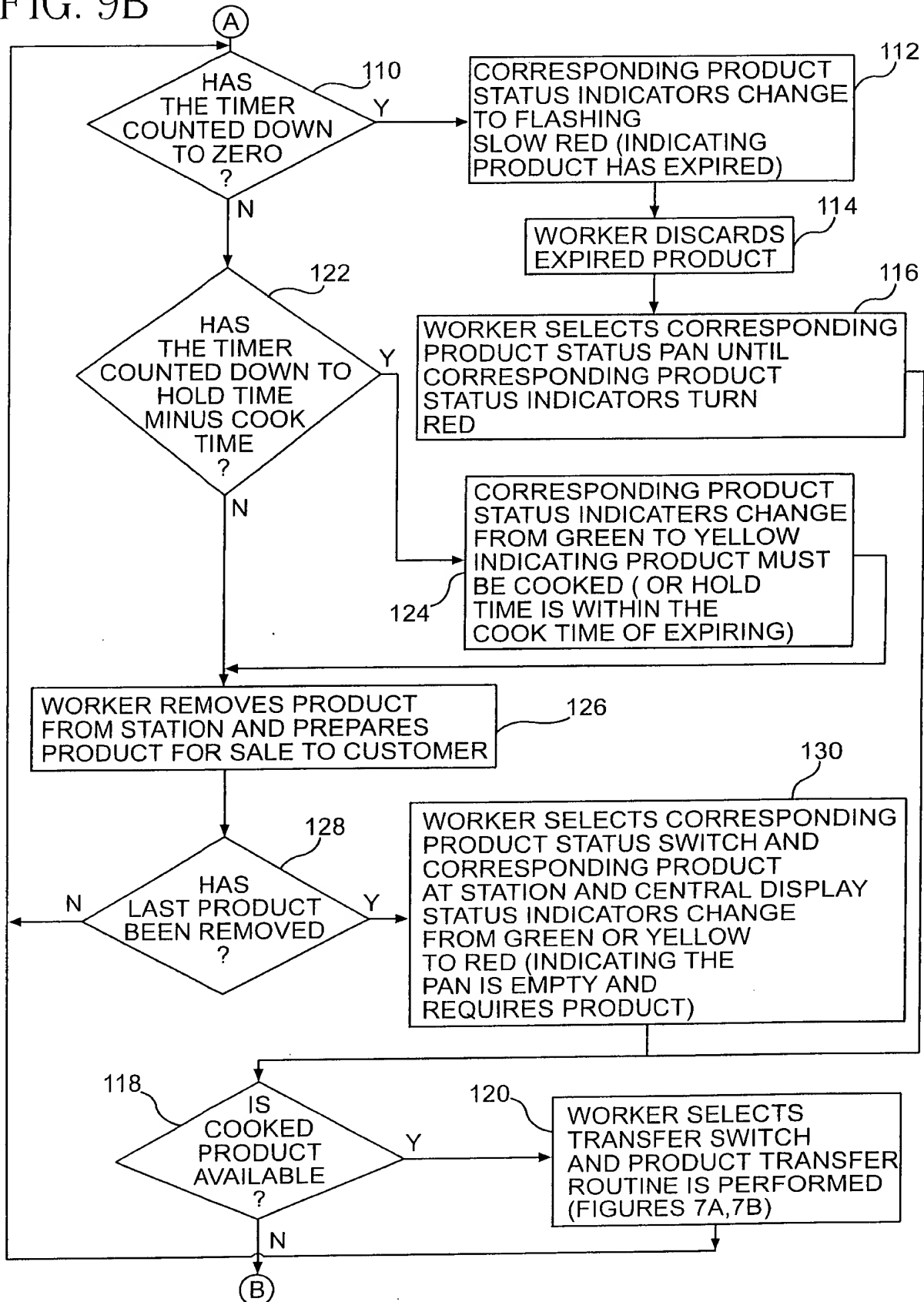
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FIG. 9A



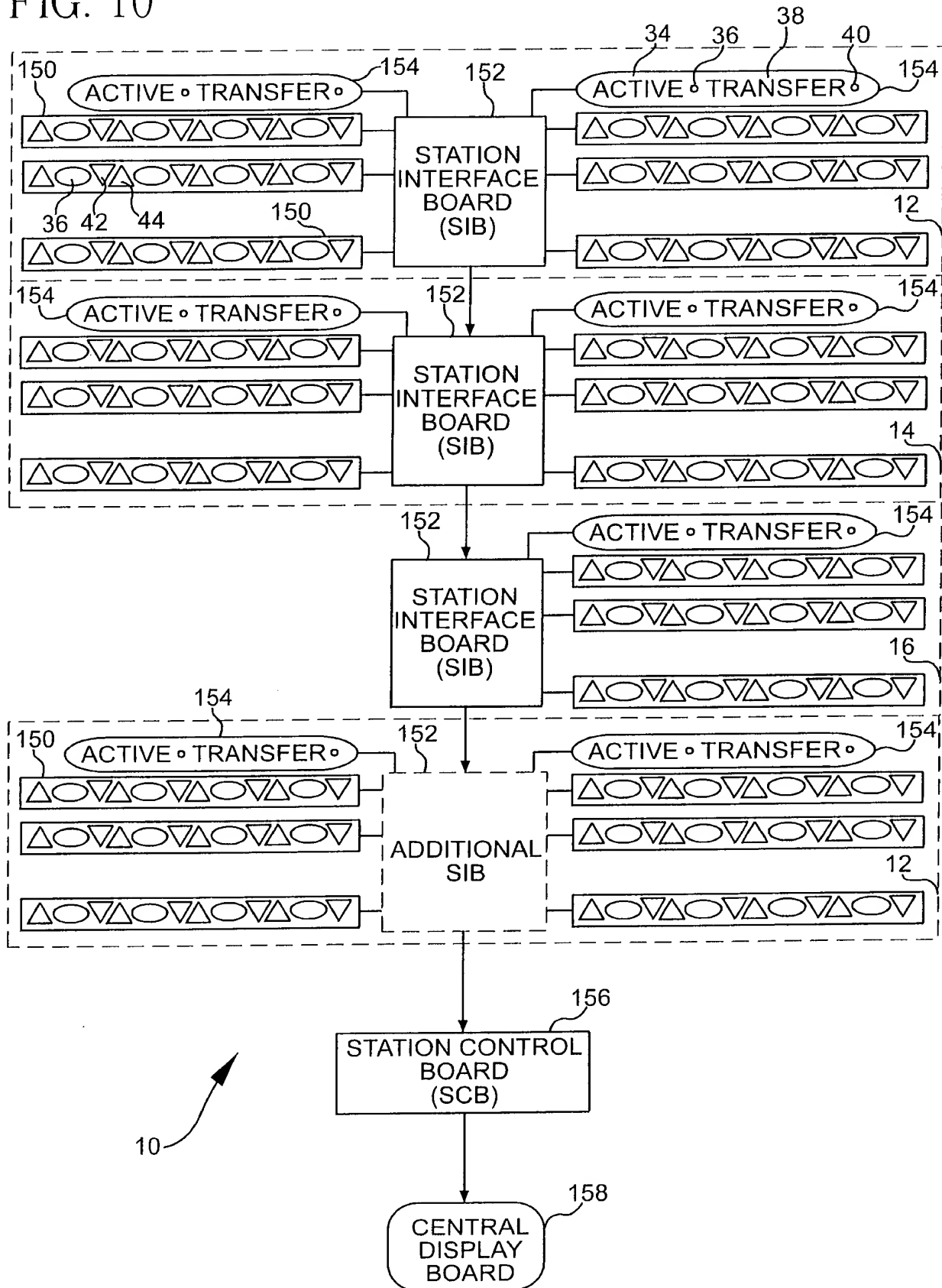
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FIG. 9B



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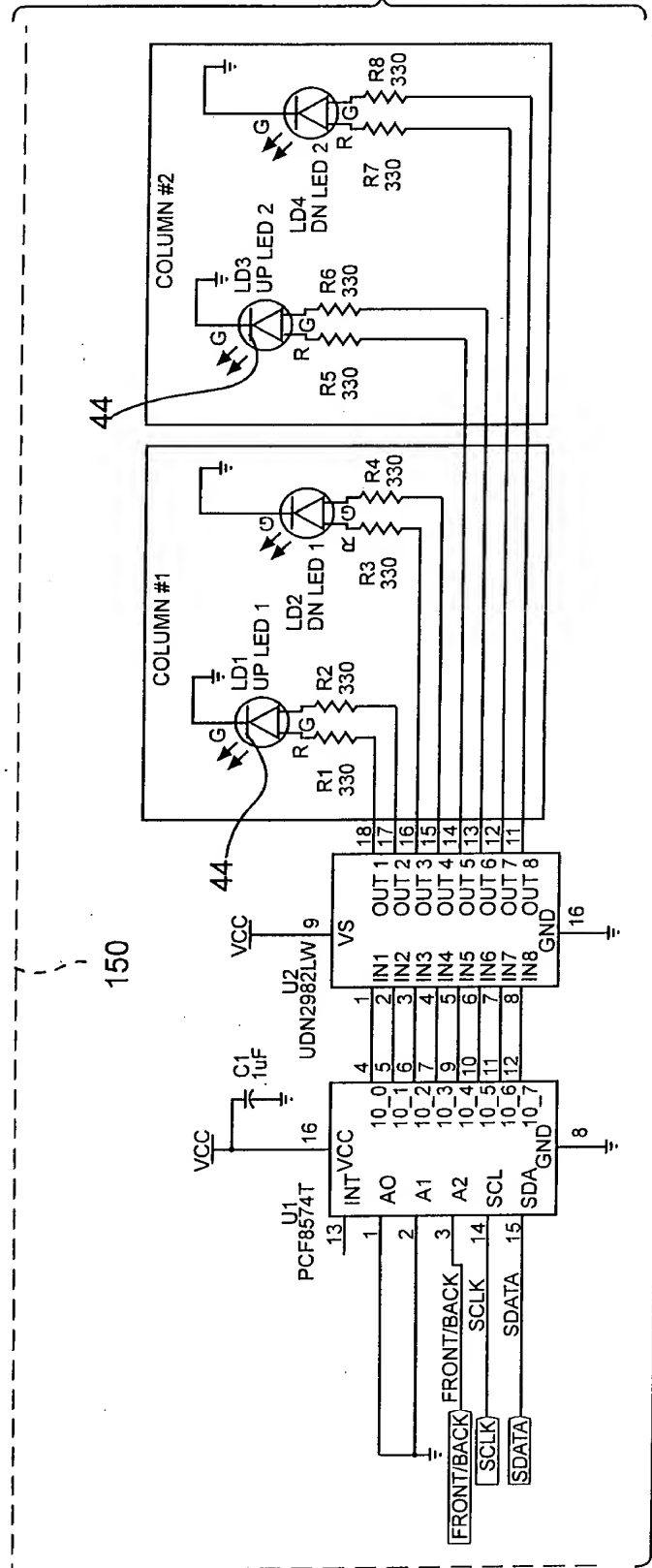
FIG. 10



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TO
FIG. 11B

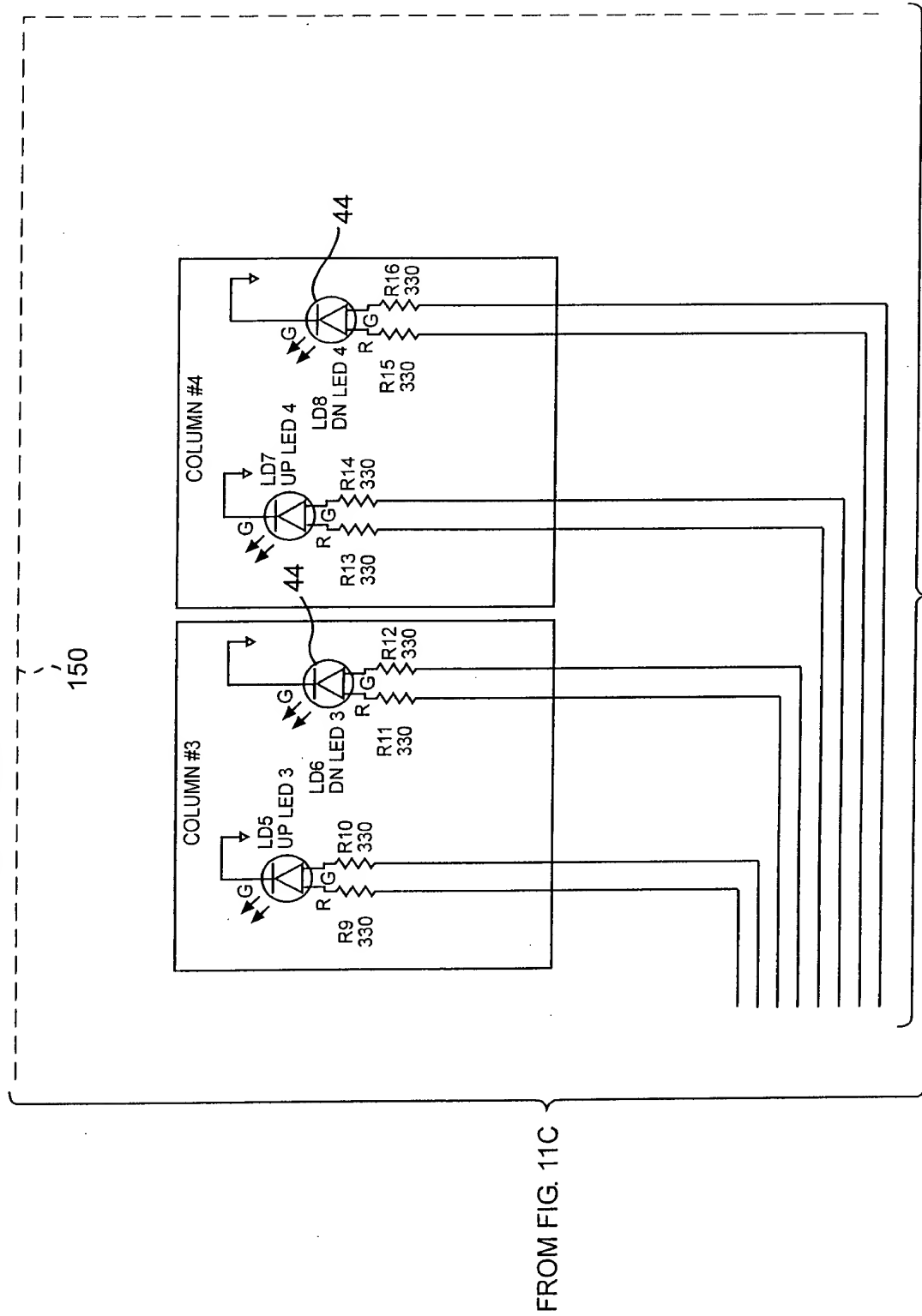
FIG. 11A STATION / WORKER INTERFACE BOARD



TO
FIG. 11C

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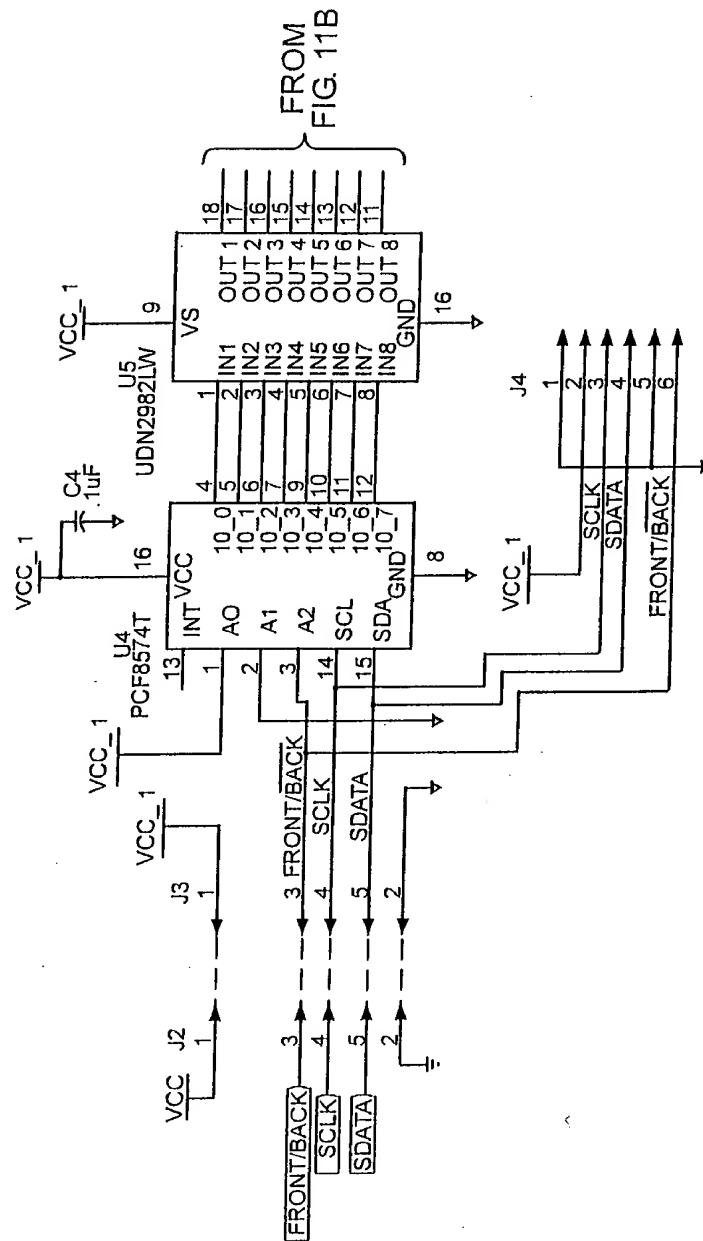
FIG. 11B STATION / WORKER INTERFACE BOARD



T0
FIG. 11E

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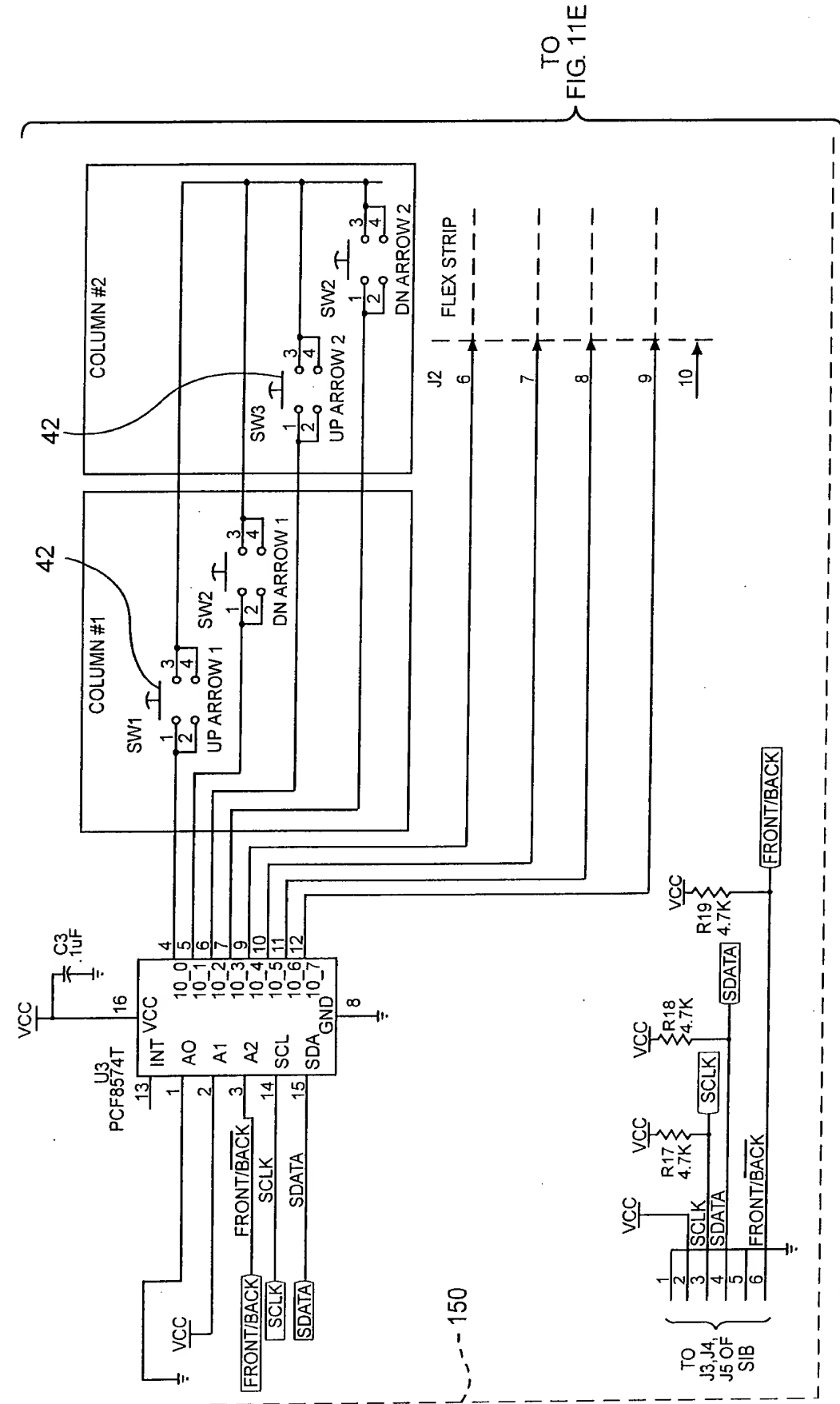
FIG. 11C STATION / WORKER INTERFACE BOARD



TO
FIG. 11E

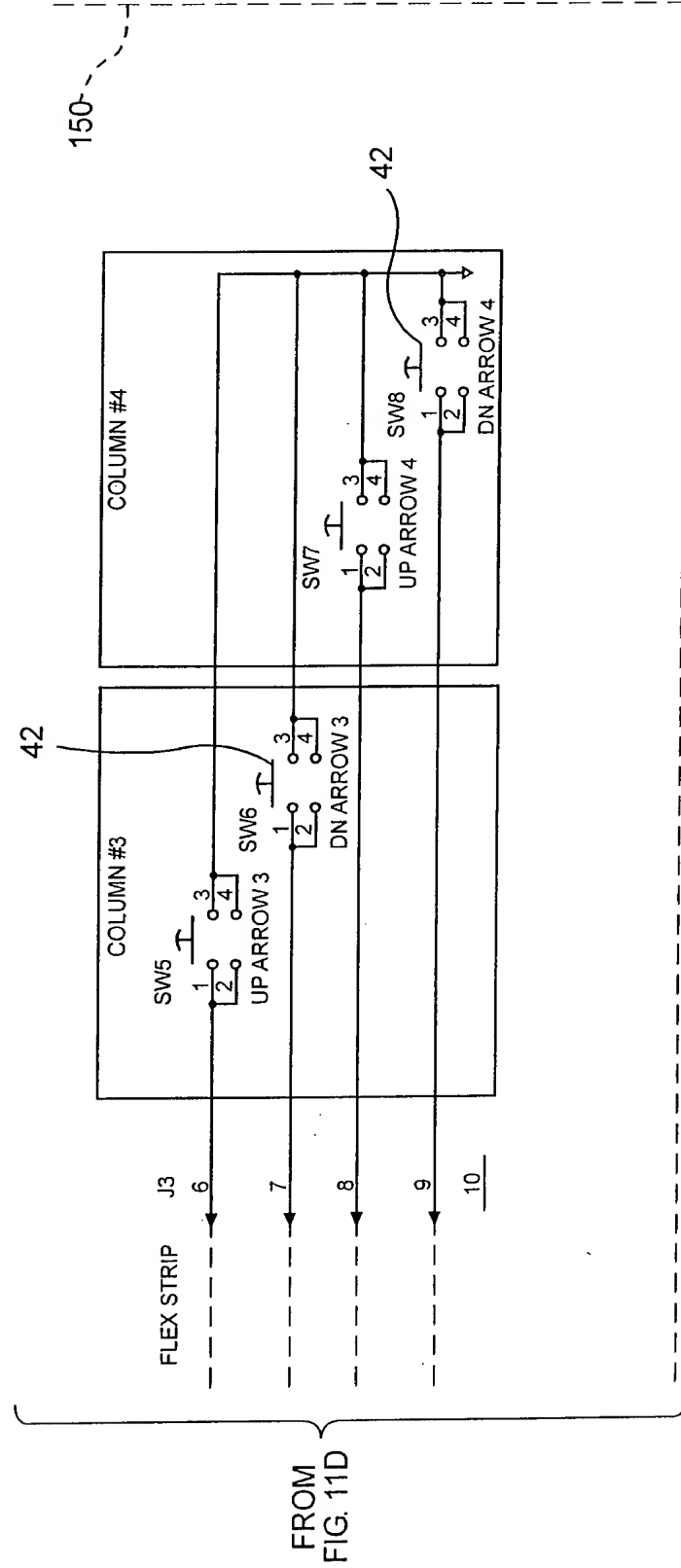
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FIG. 11D STATION / WORKER INTERFACE BOARD



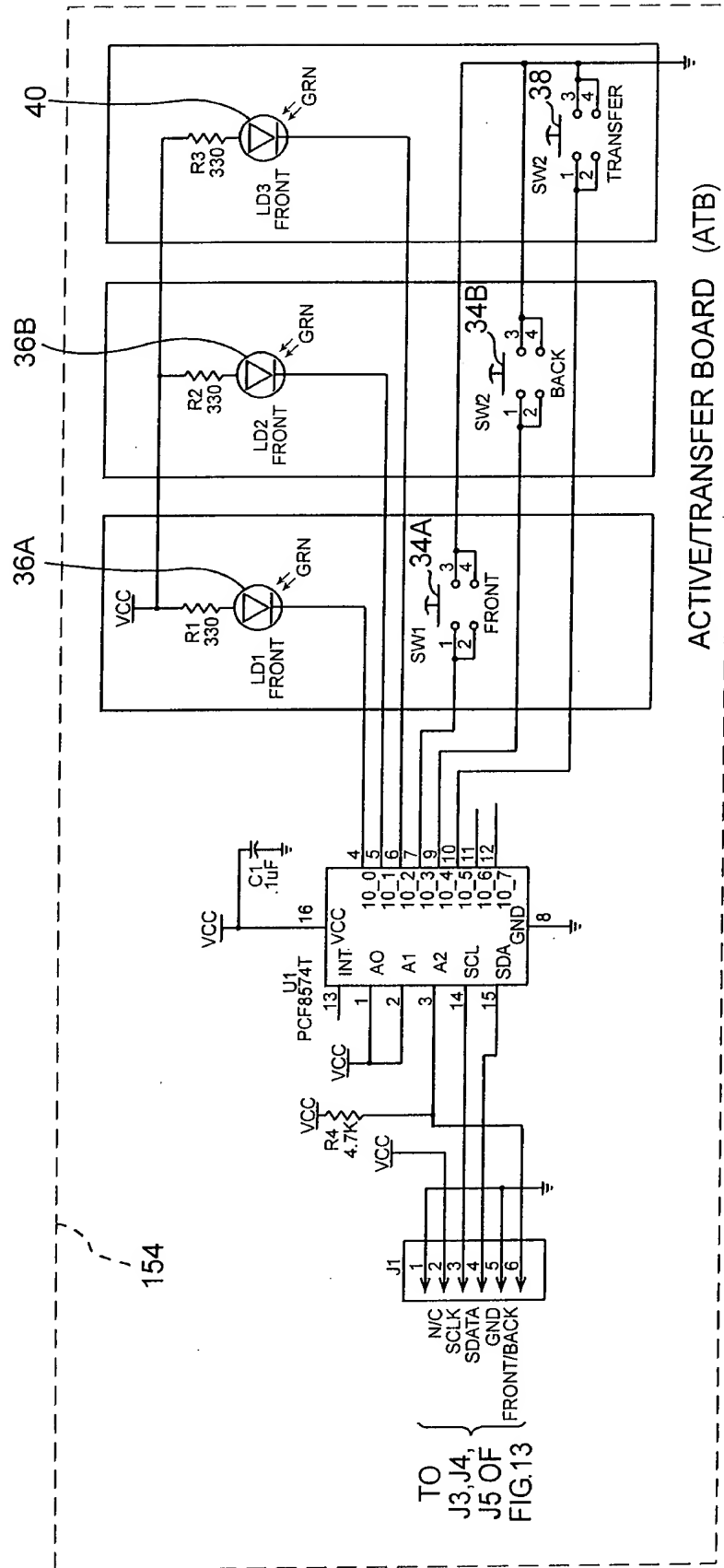
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FIG. 11E STATION / WORKER INTERFACE BOARD

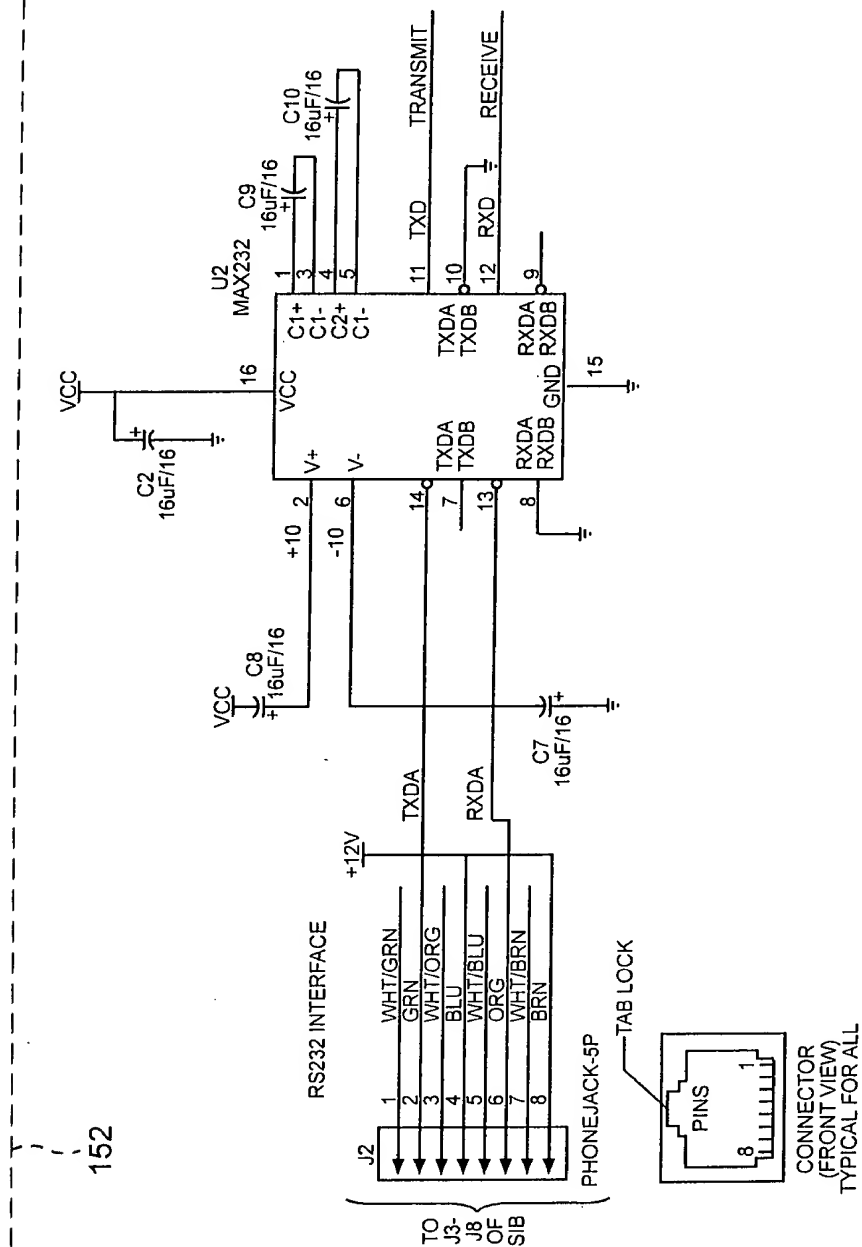


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FIG. 12



TO
FIG. 13B



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FIG. 13B STATION INTERFACE BOARD (SIB)

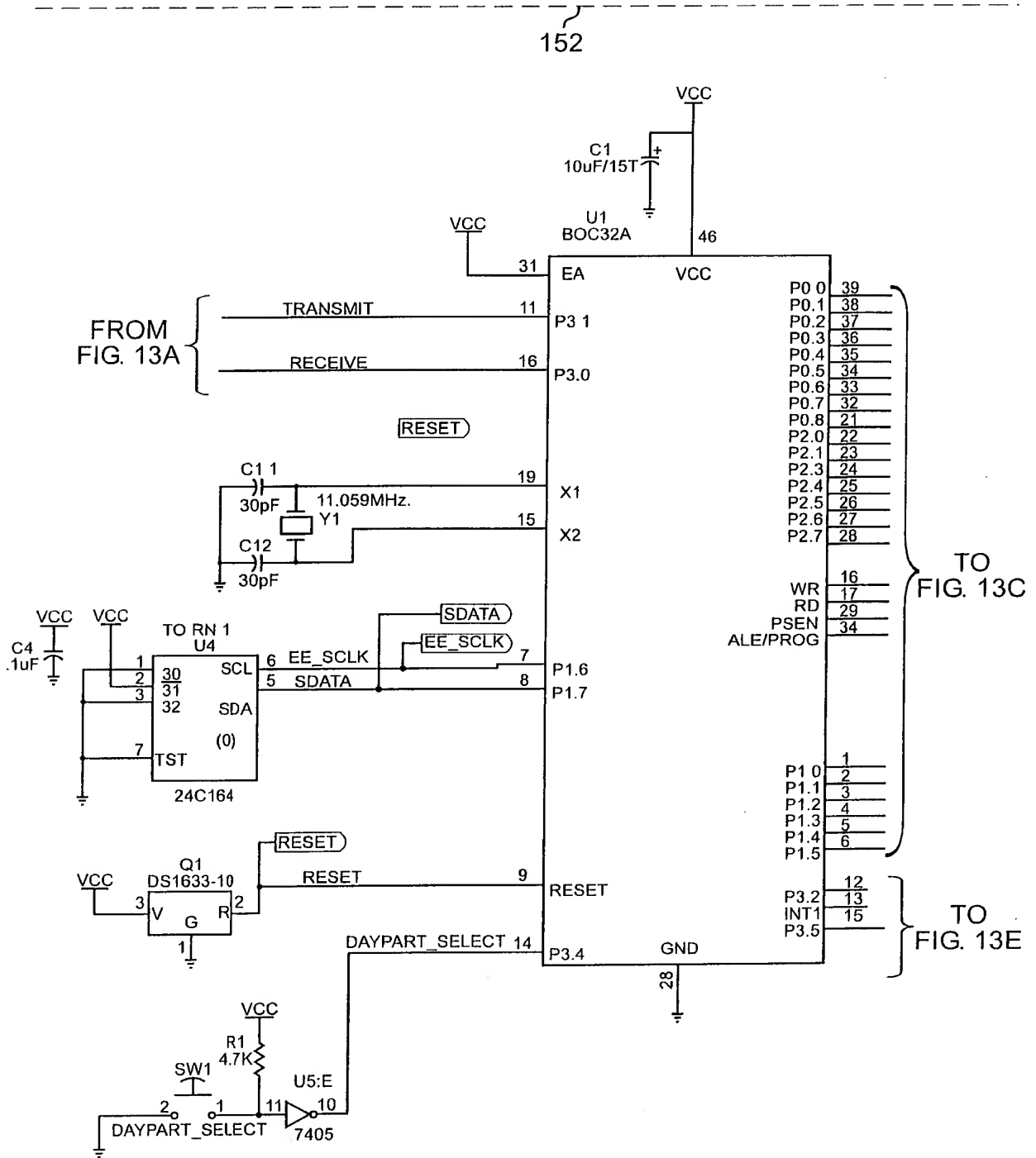
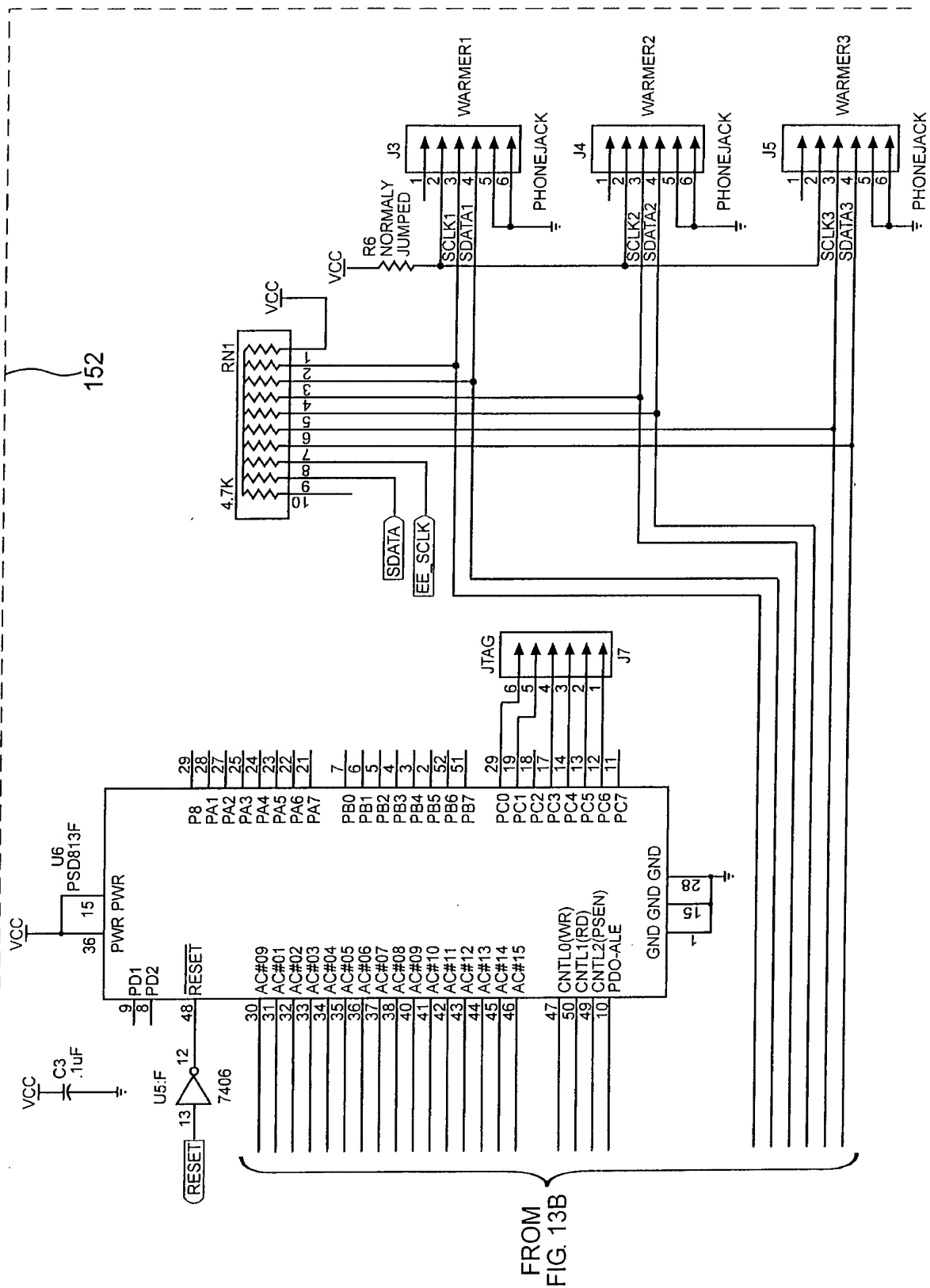
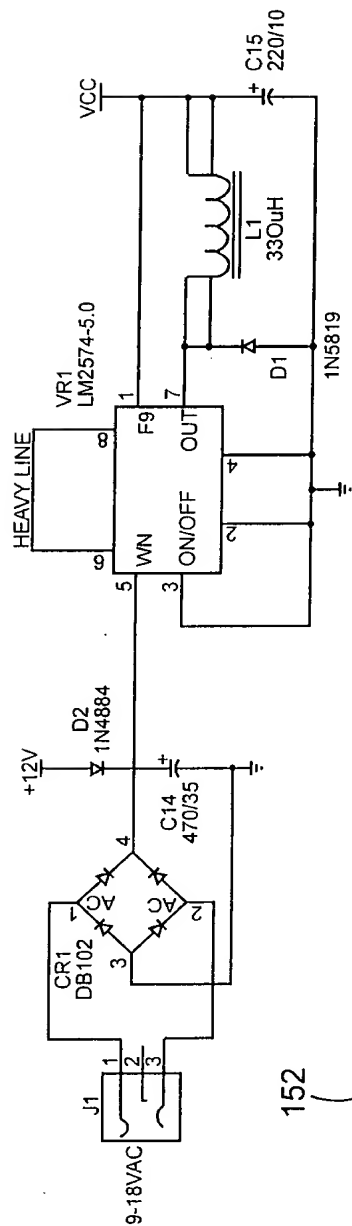


FIG. 13C STATION INTERFACE BOARD (SIB)



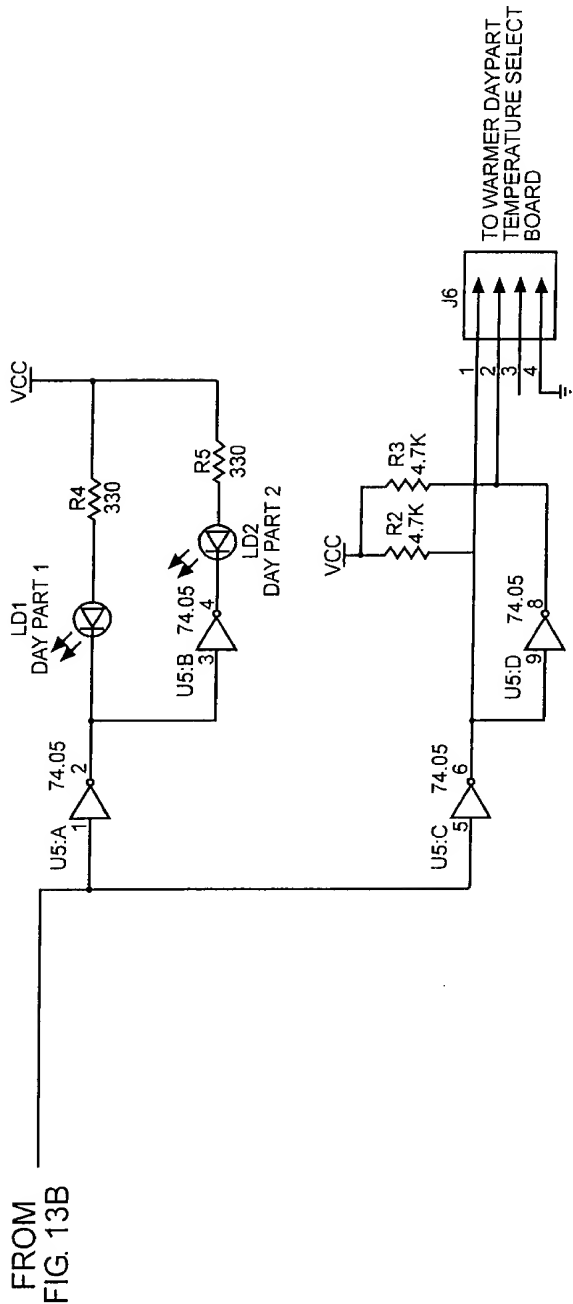
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FIG. 13D STATION INTERFACE BOARD (SIB)



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FIG. 13E STATION INTERFACE BOARD (SIB)



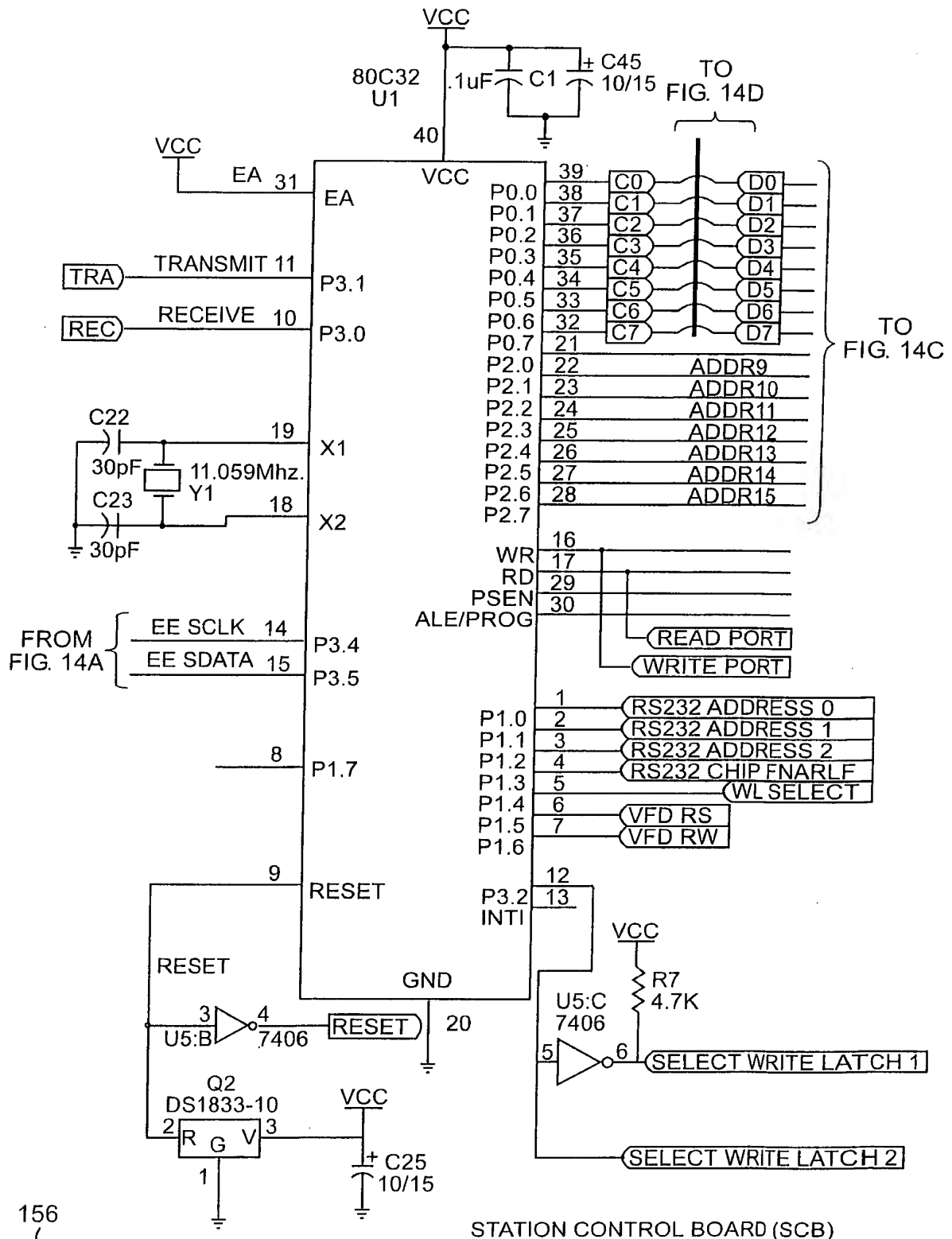
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The schematic diagram illustrates the hardware for the 24C154. It features two 24C154 chips, U6 and U7, which are connected to a PCF8570 (U15) and a PCF8583 (U14). The 24C154 chips are configured with S0, S1, and S2 pins connected to VCC, and TST pins connected to GND. The PCF8570 (U15) is connected to VCC and GND, with its SCL and SDA pins connected to the 24C154 chips. The PCF8583 (U14) is connected to VCC and GND, with its SCL and SDA pins connected to the 24C154 chips. The diagram also shows a 32.768KHz crystal (Y2) connected to the PCF8583, and various capacitors (C15, C14, C29, C25) used for timing and decoupling. The power supply is VCC, and the ground is GND.

TO
FIG. 14B

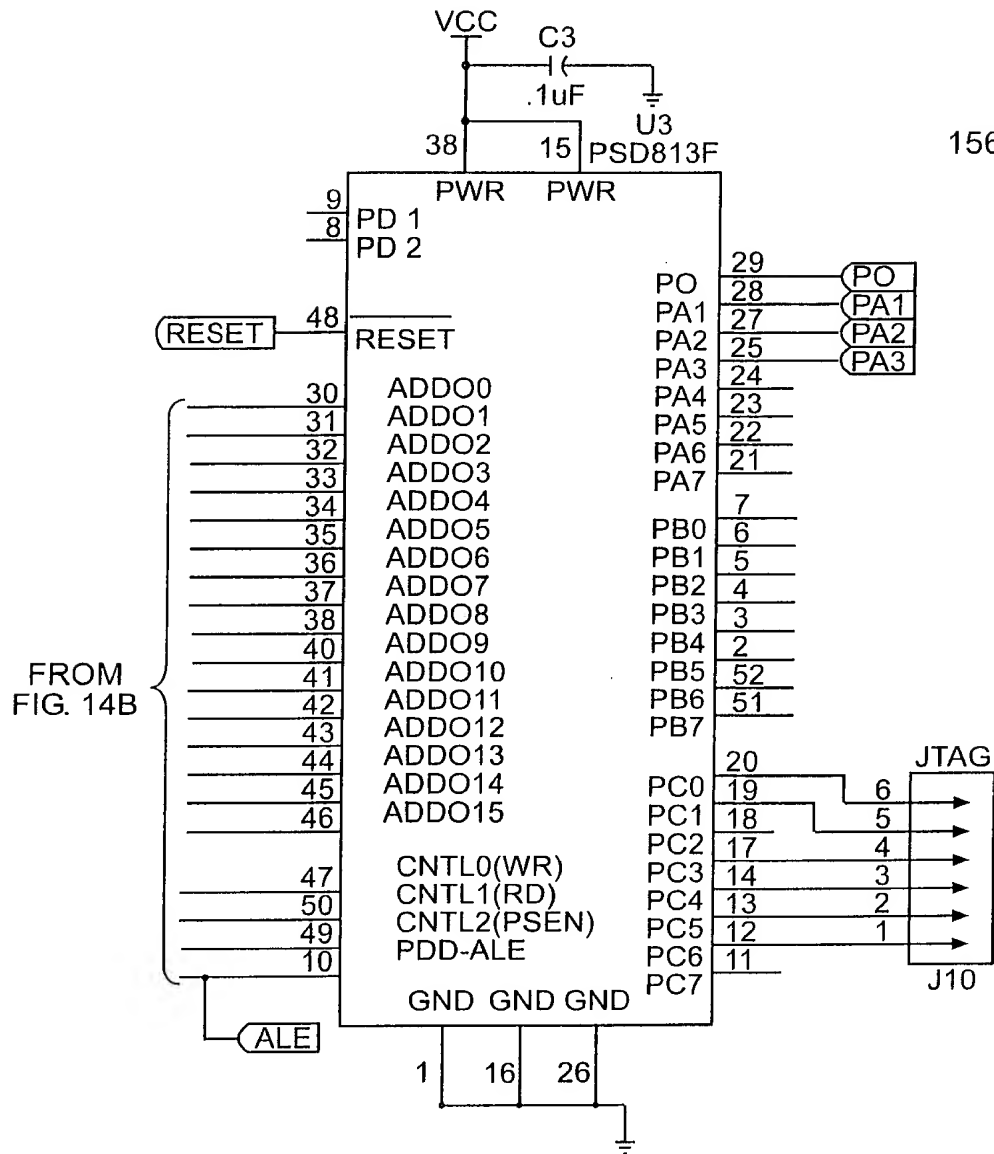
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FIG. 14B STATION CONTROL BOARD (SCB)



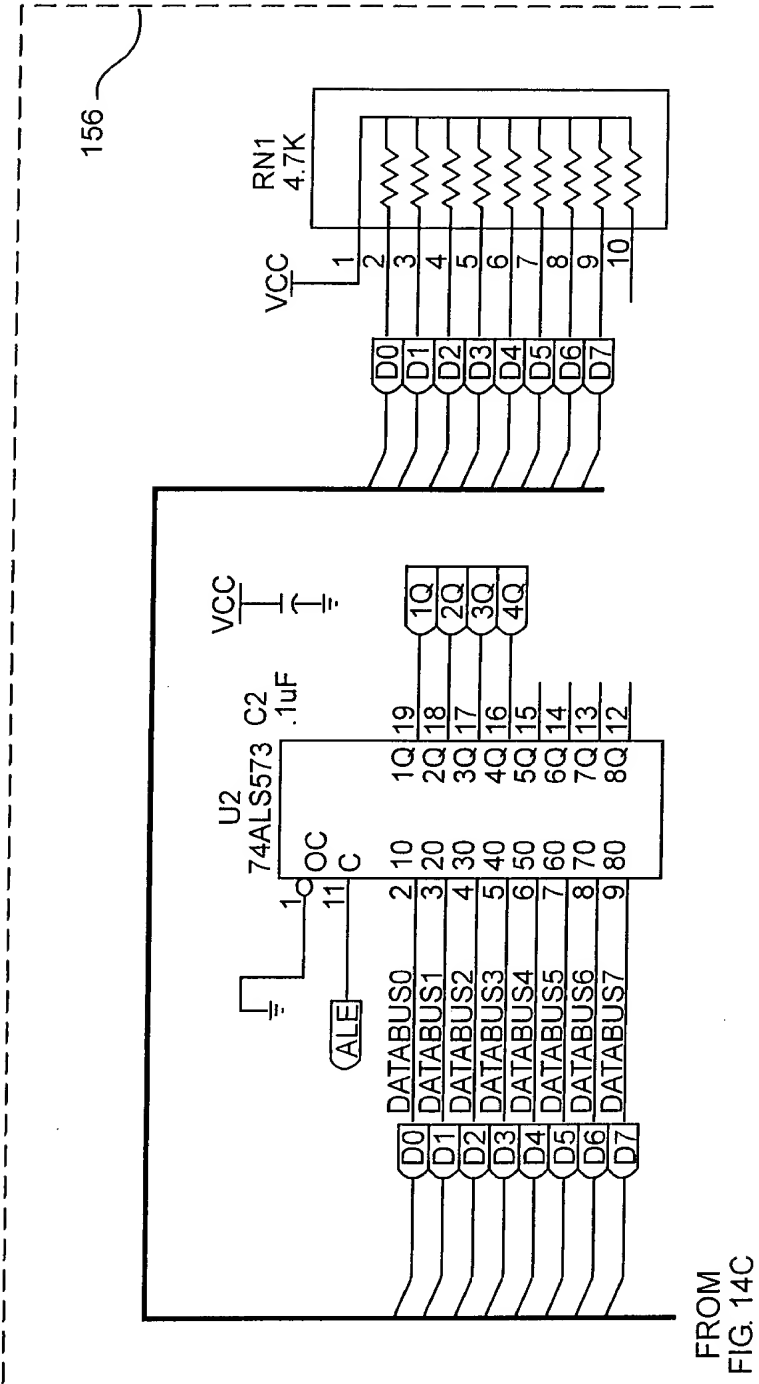
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FIG. 14C STATION CONTROL BOARD (SCB)



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FIG. 14D STATION CONTROL BOARD (SCB)



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FIG. 14E STATION CONTROL BOARD (SCB)

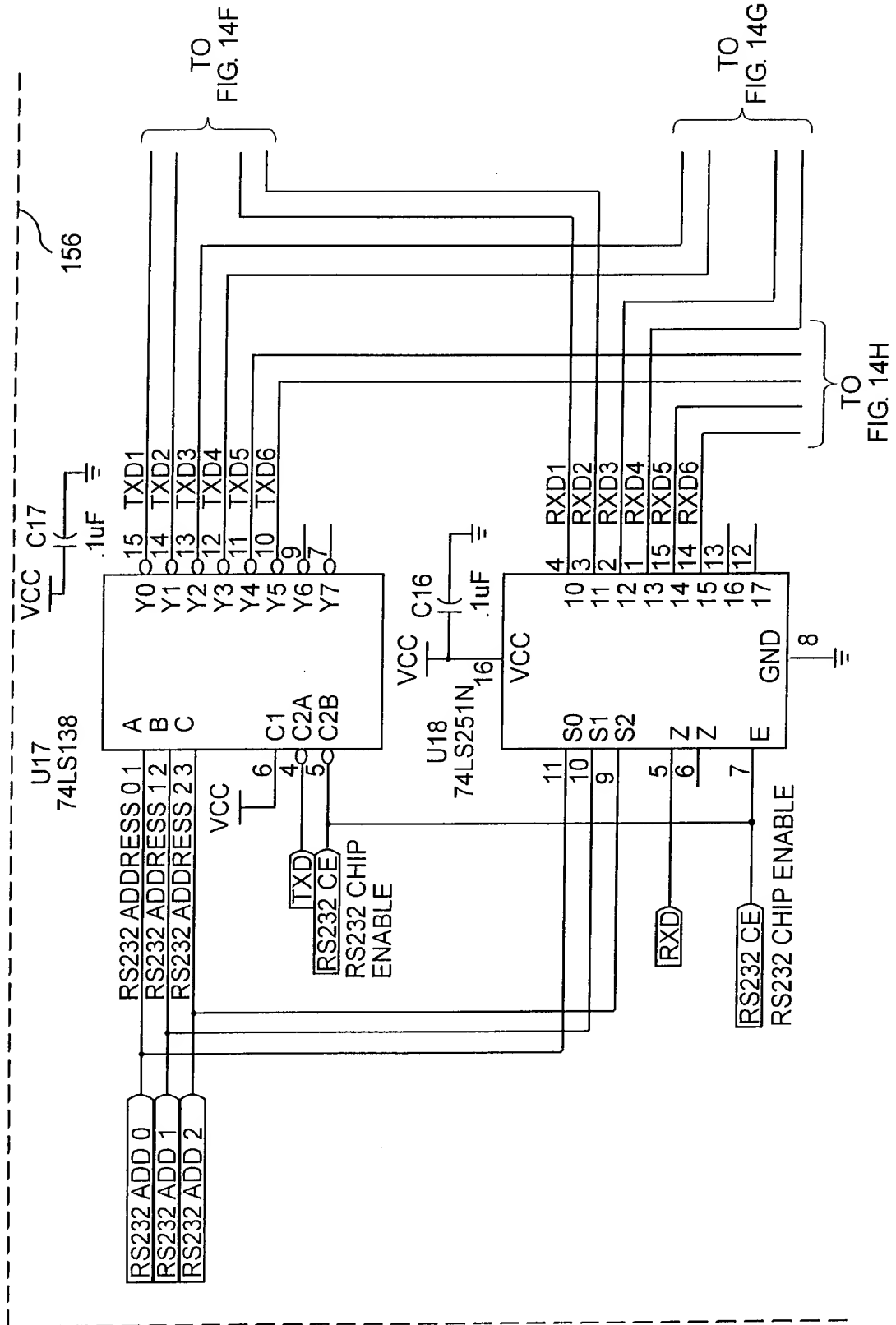
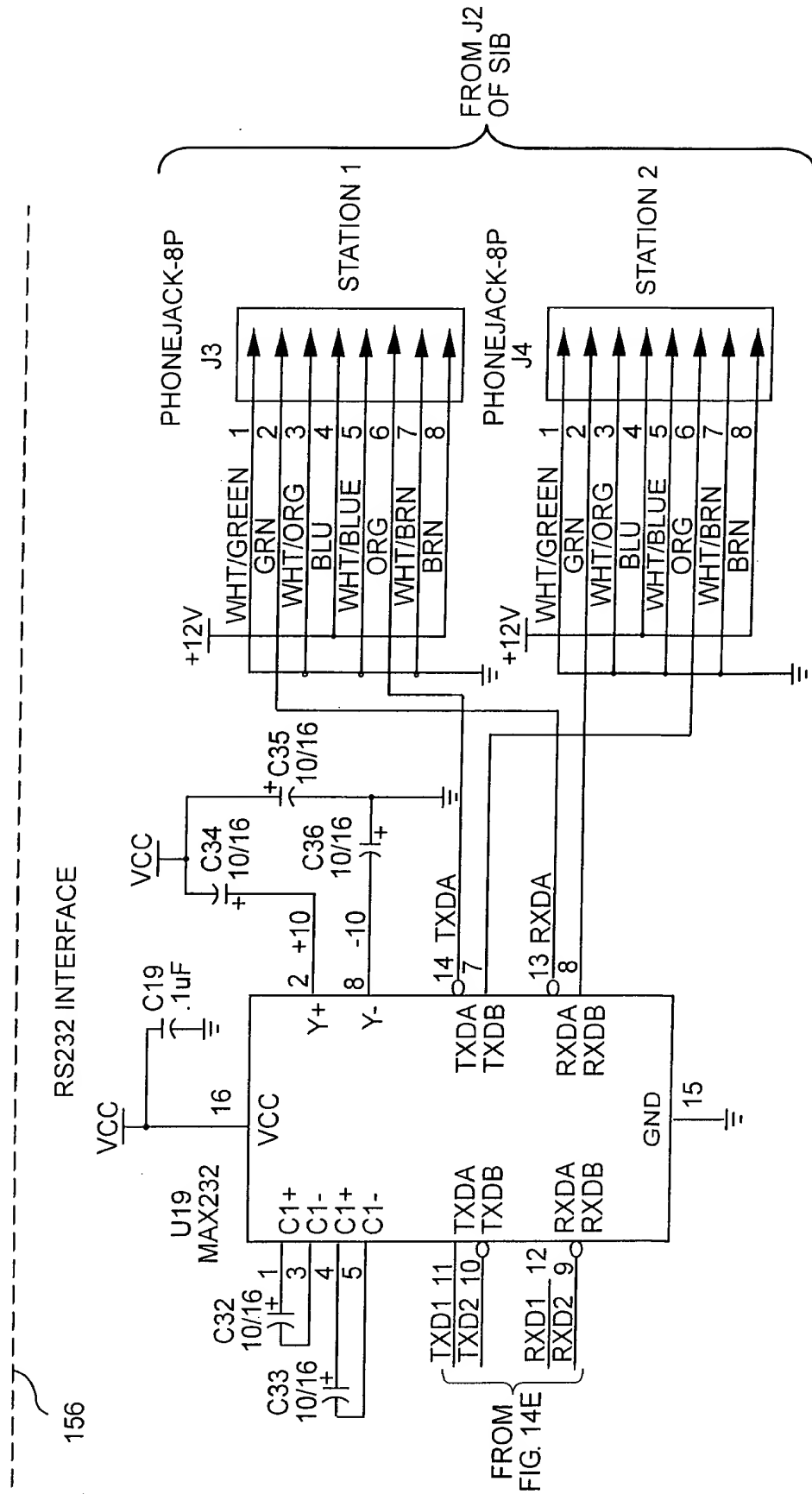
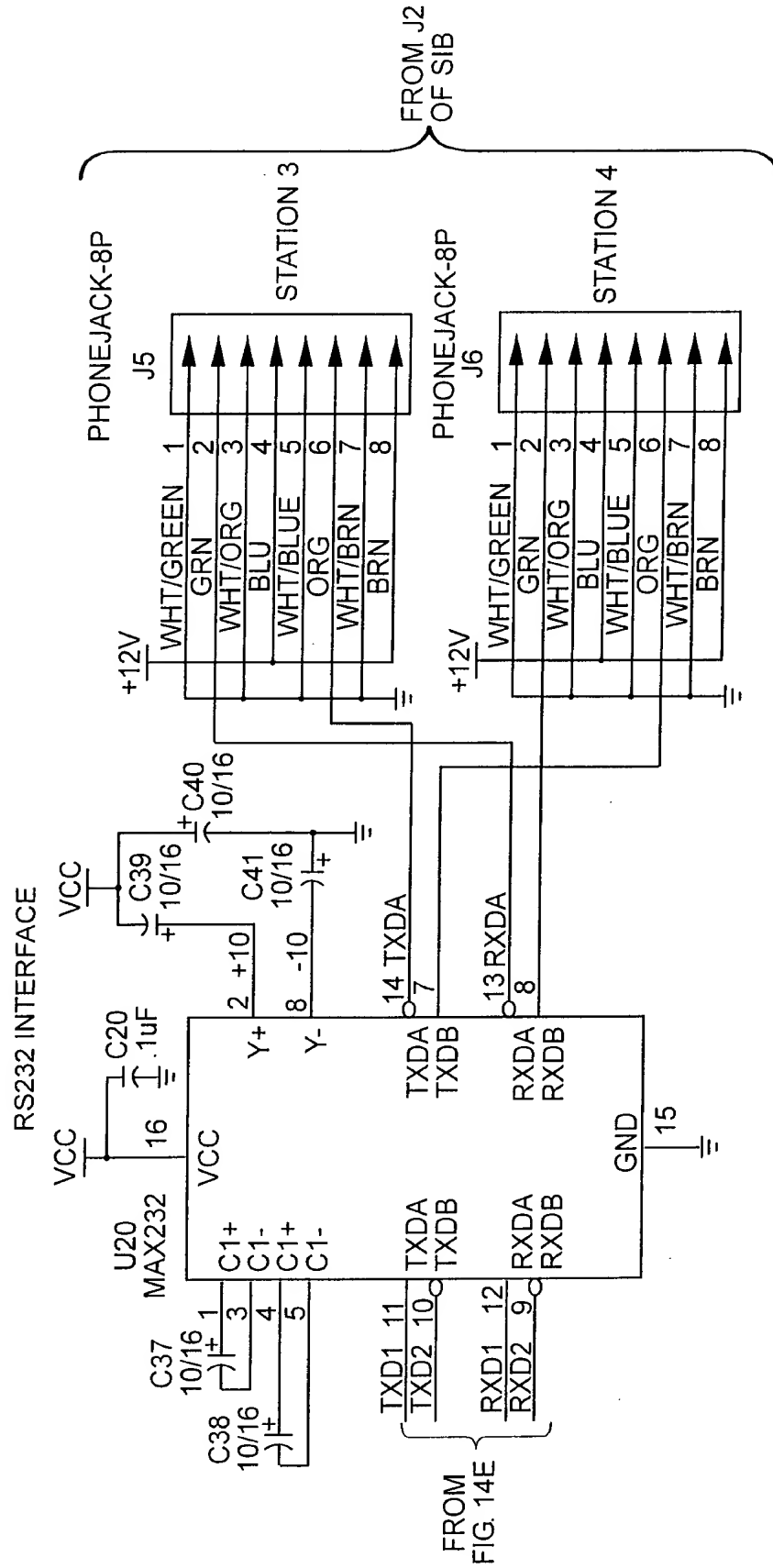


FIG. 14F STATION CONTROL BOARD (SCB)



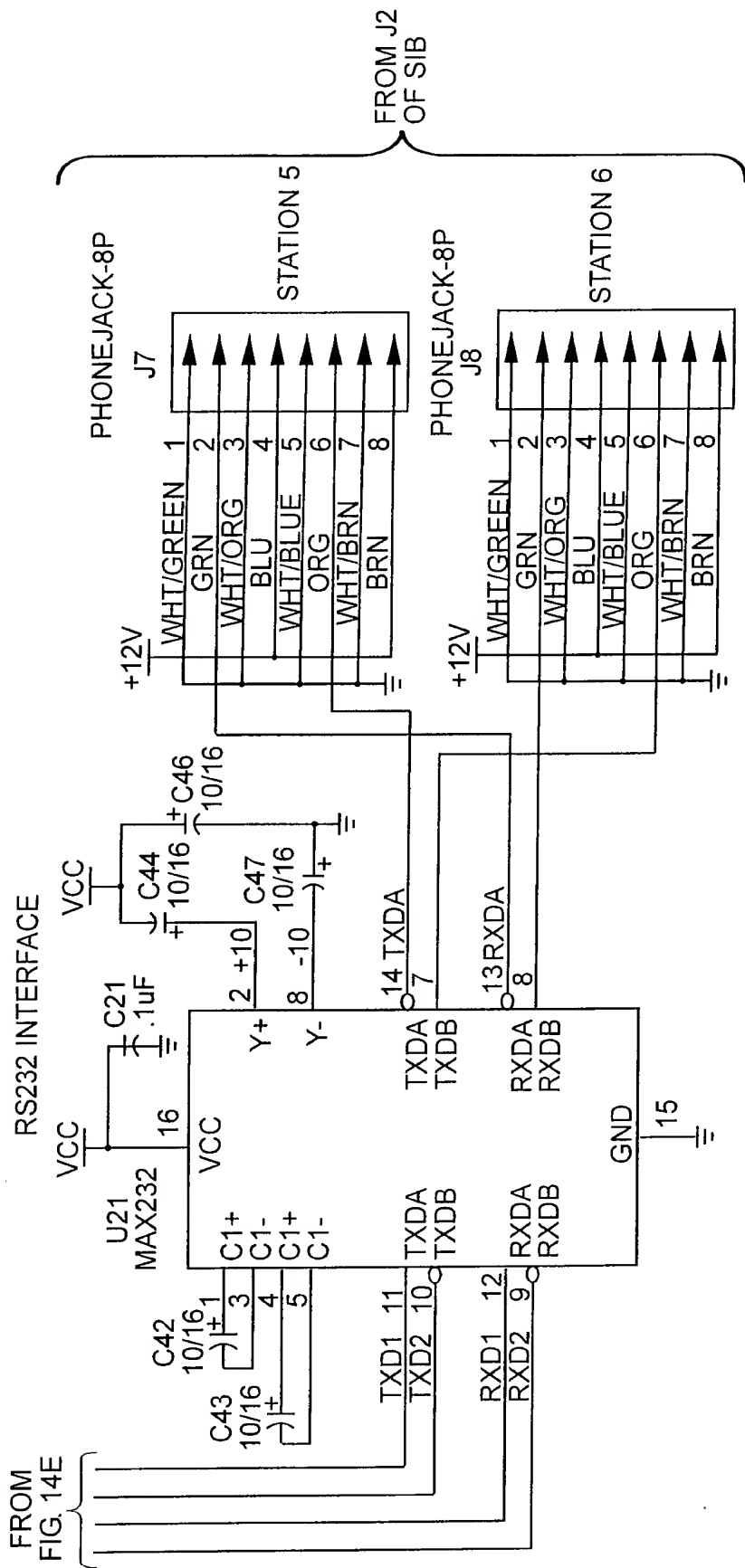
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FIG. 14G STATION CONTROL BOARD (SCB)



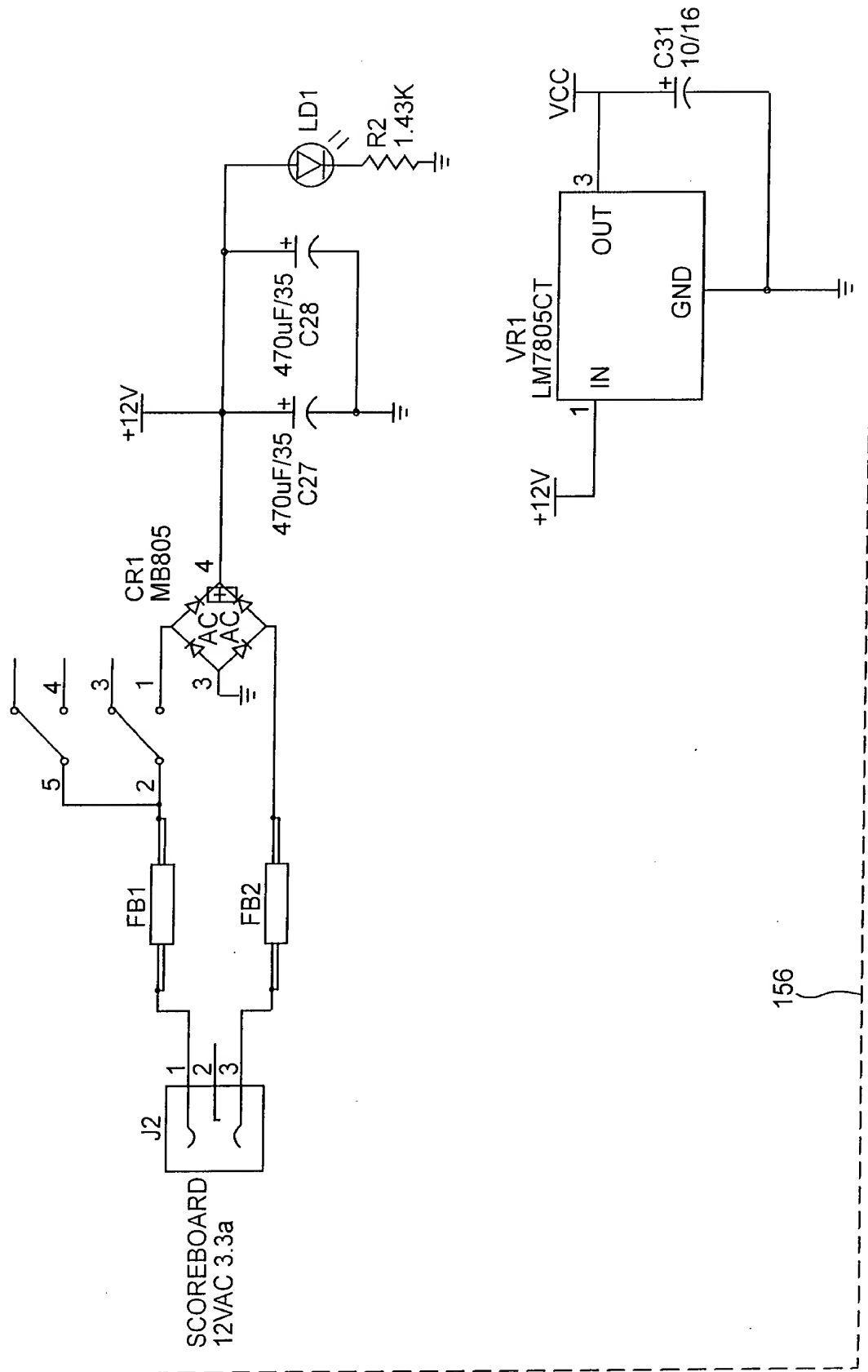
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FIG. 14H STATION CONTROL BOARD (SCB)



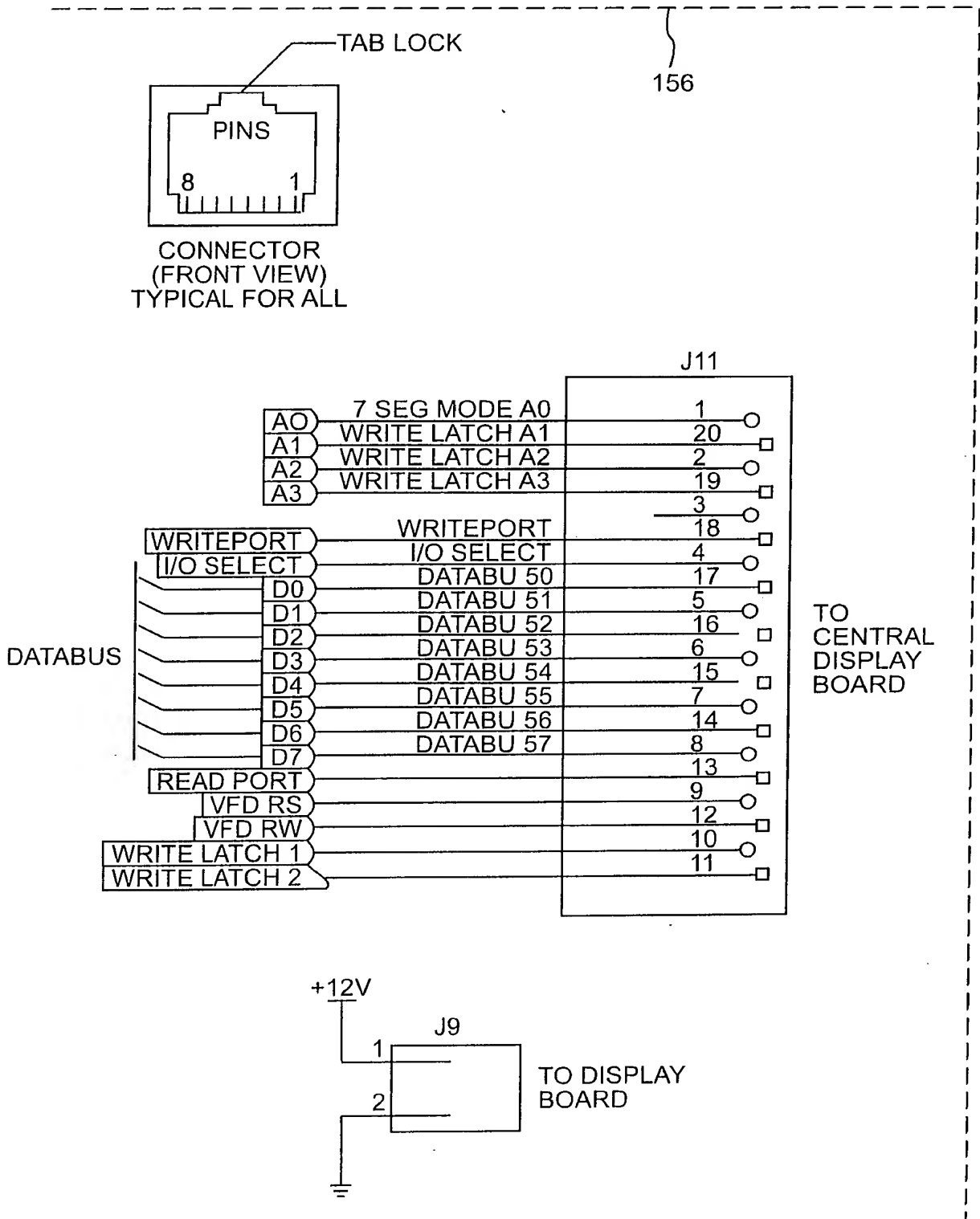
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FIG. 14I STATION CONTROL BOARD (SCB)



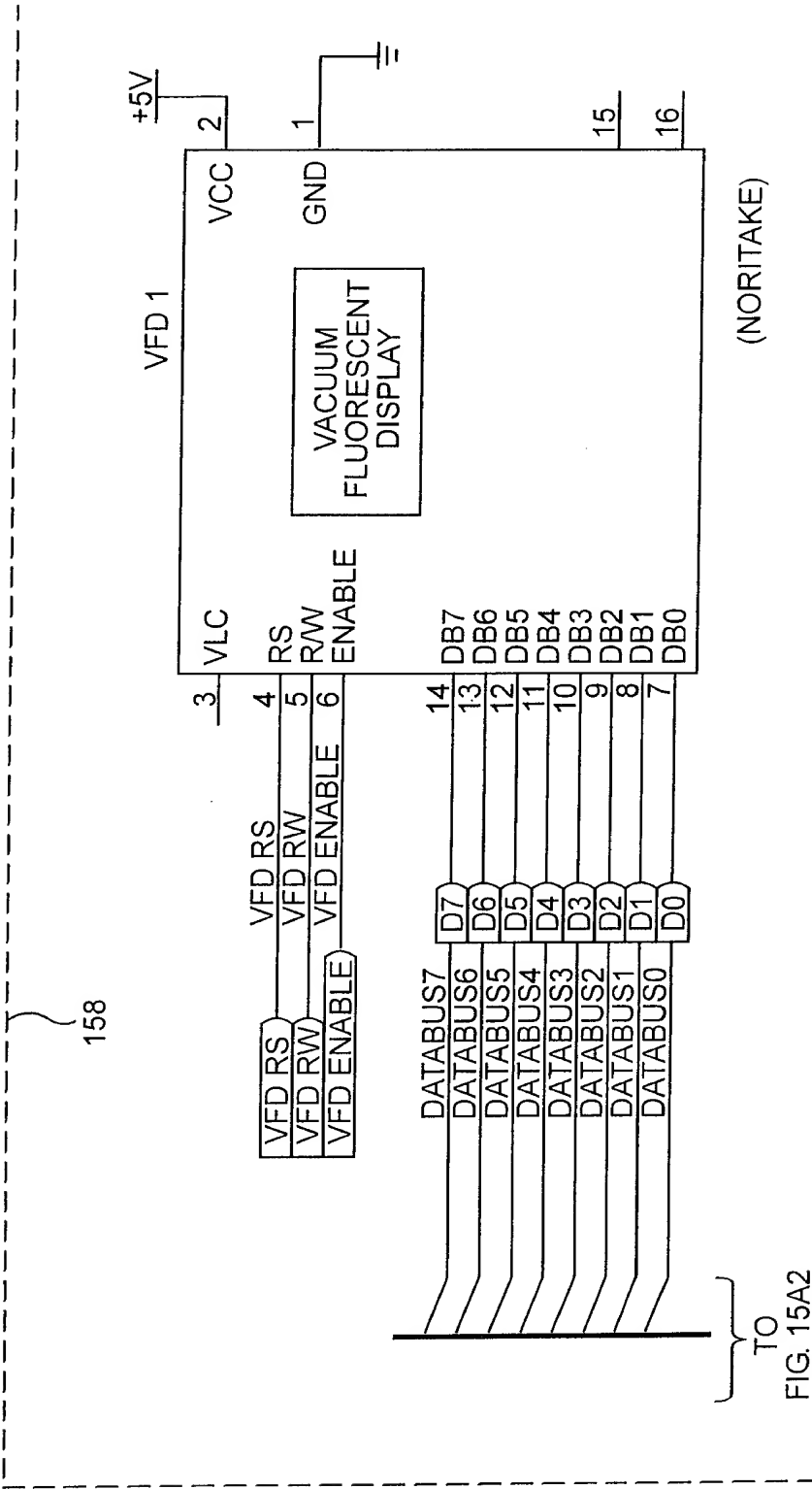
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FIG. 14J STATION CONTROL BOARD (SCB)



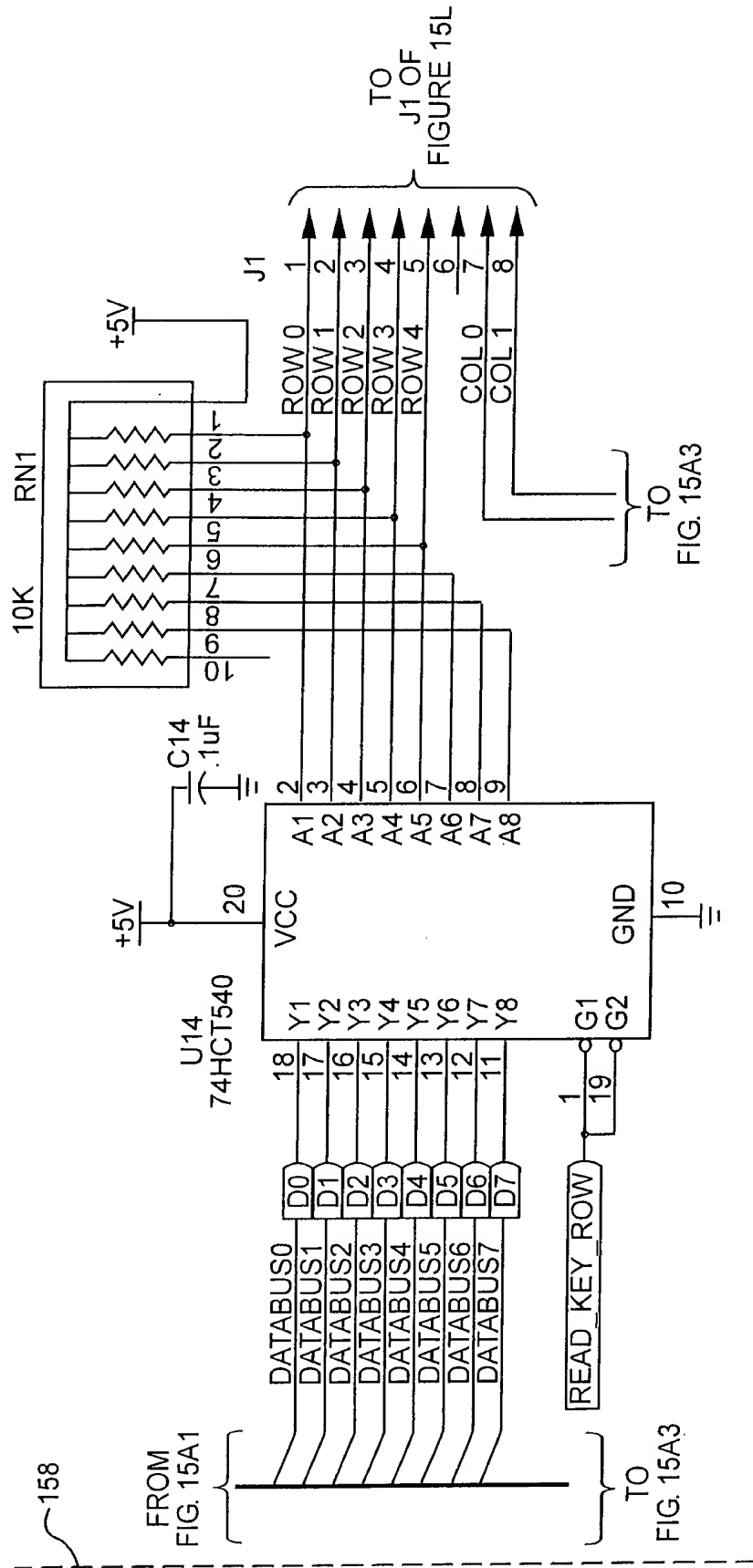
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FIG. 15A1 CENTRAL DISPLAY BOARD



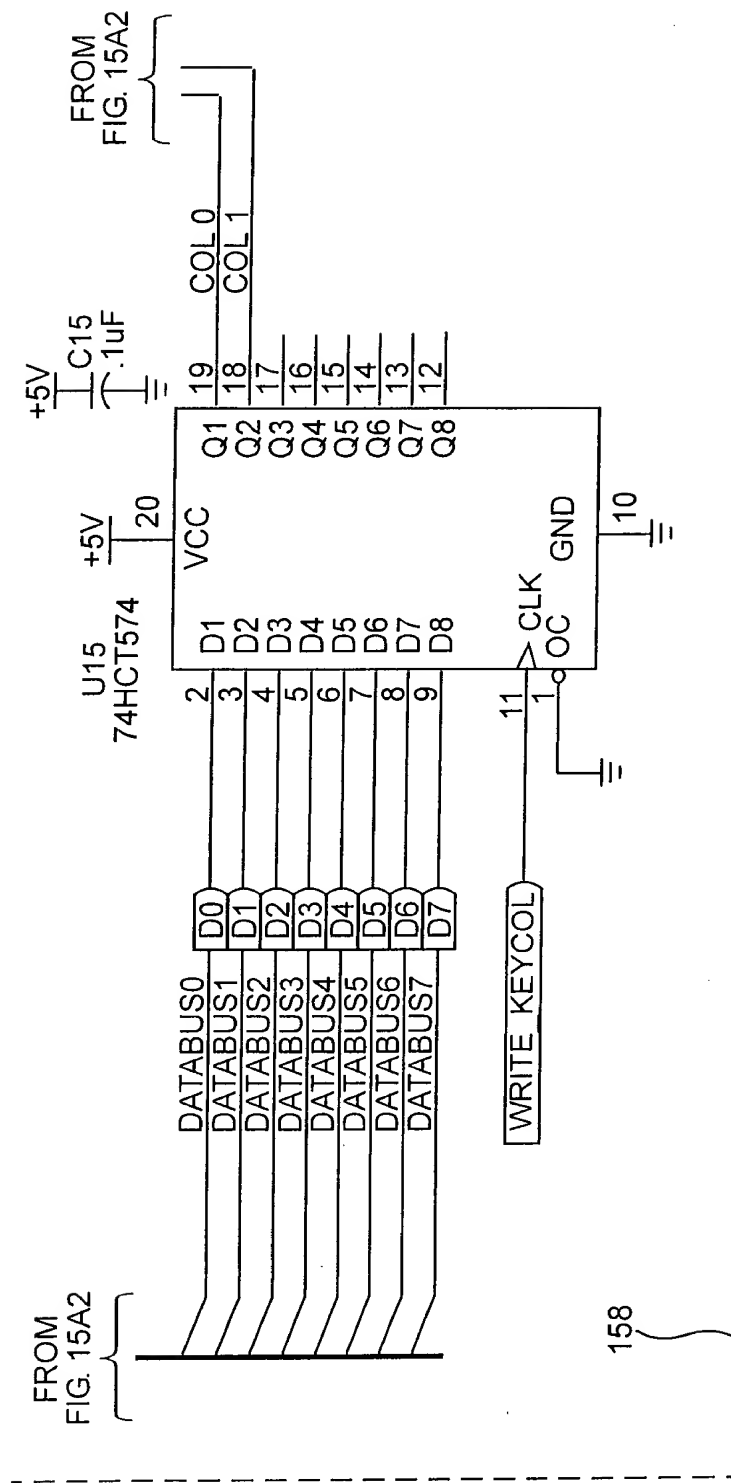
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FIG. 15A2 CENTRAL DISPLAY BOARD



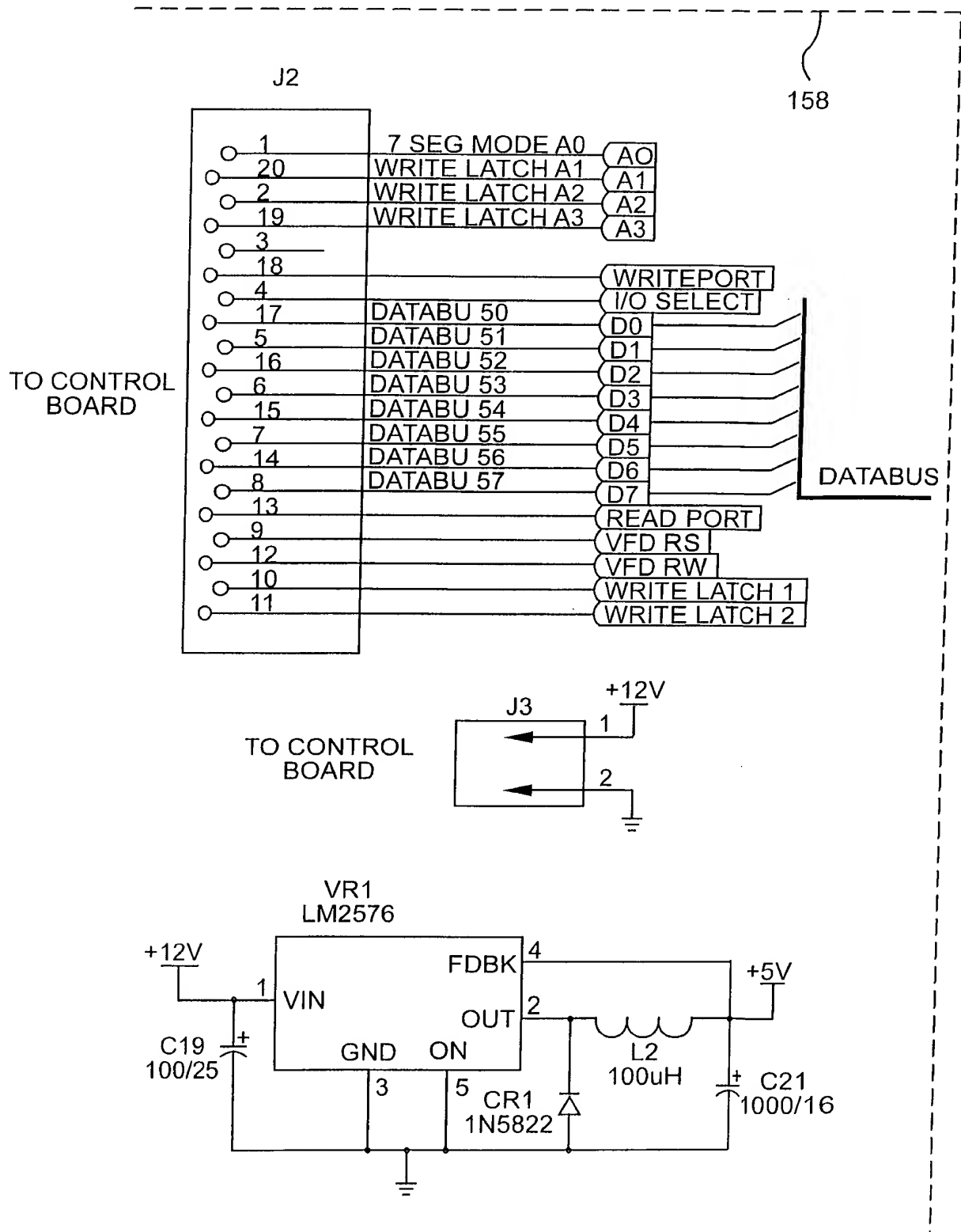
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FIG. 15A3 CENTRAL DISPLAY BOARD



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FIG. 15A4 CENTRAL DISPLAY BOARD



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FIG. 15B1 CENTRAL DISPLAY BOARD

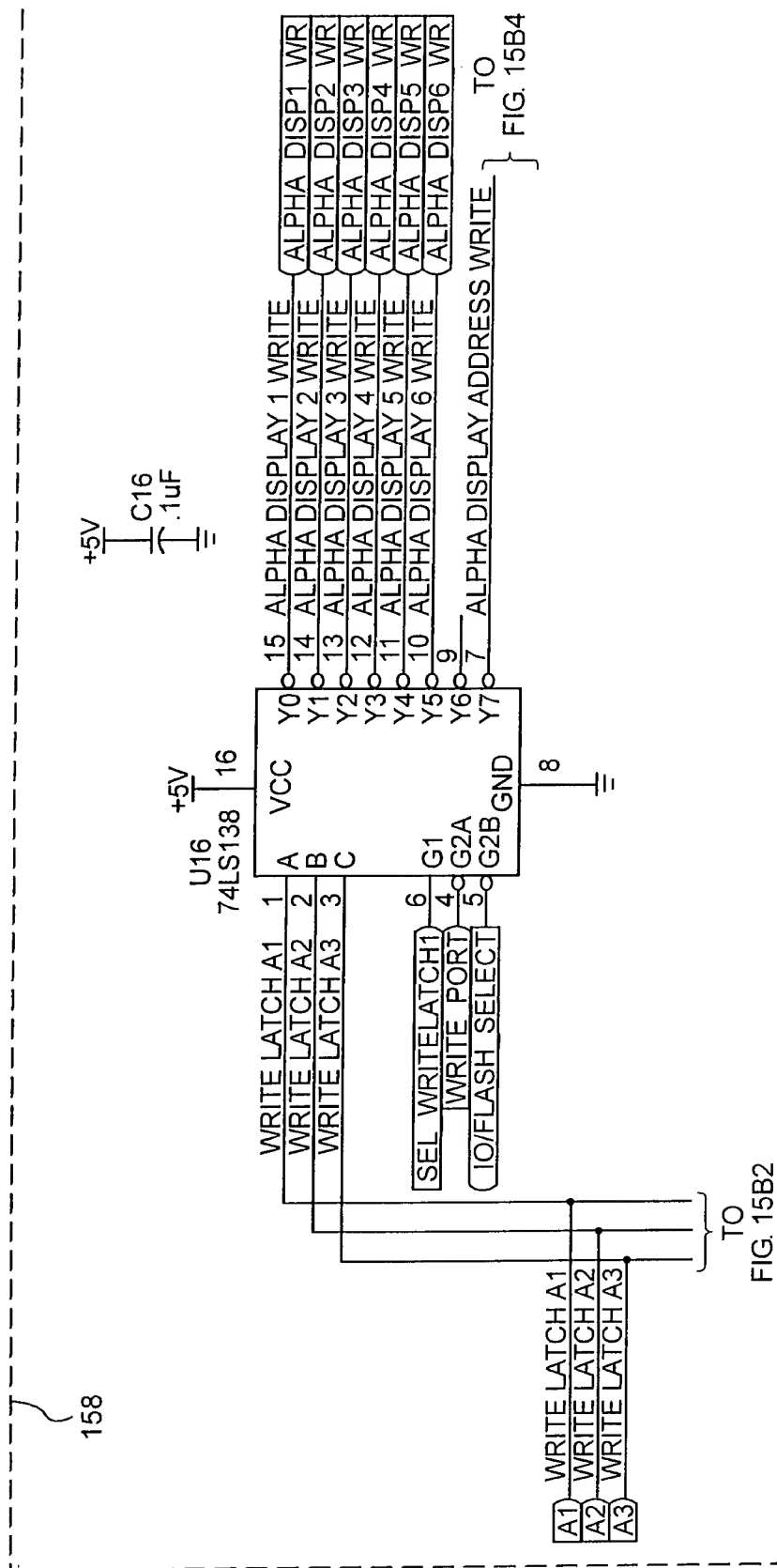
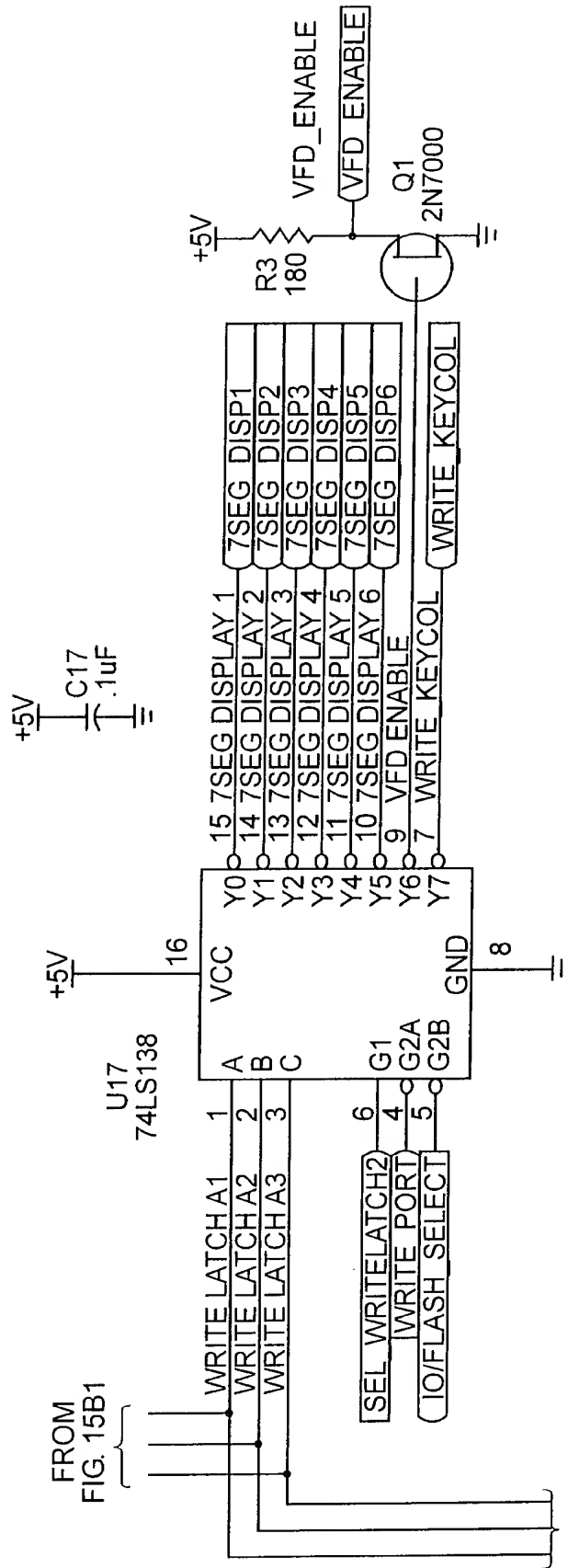
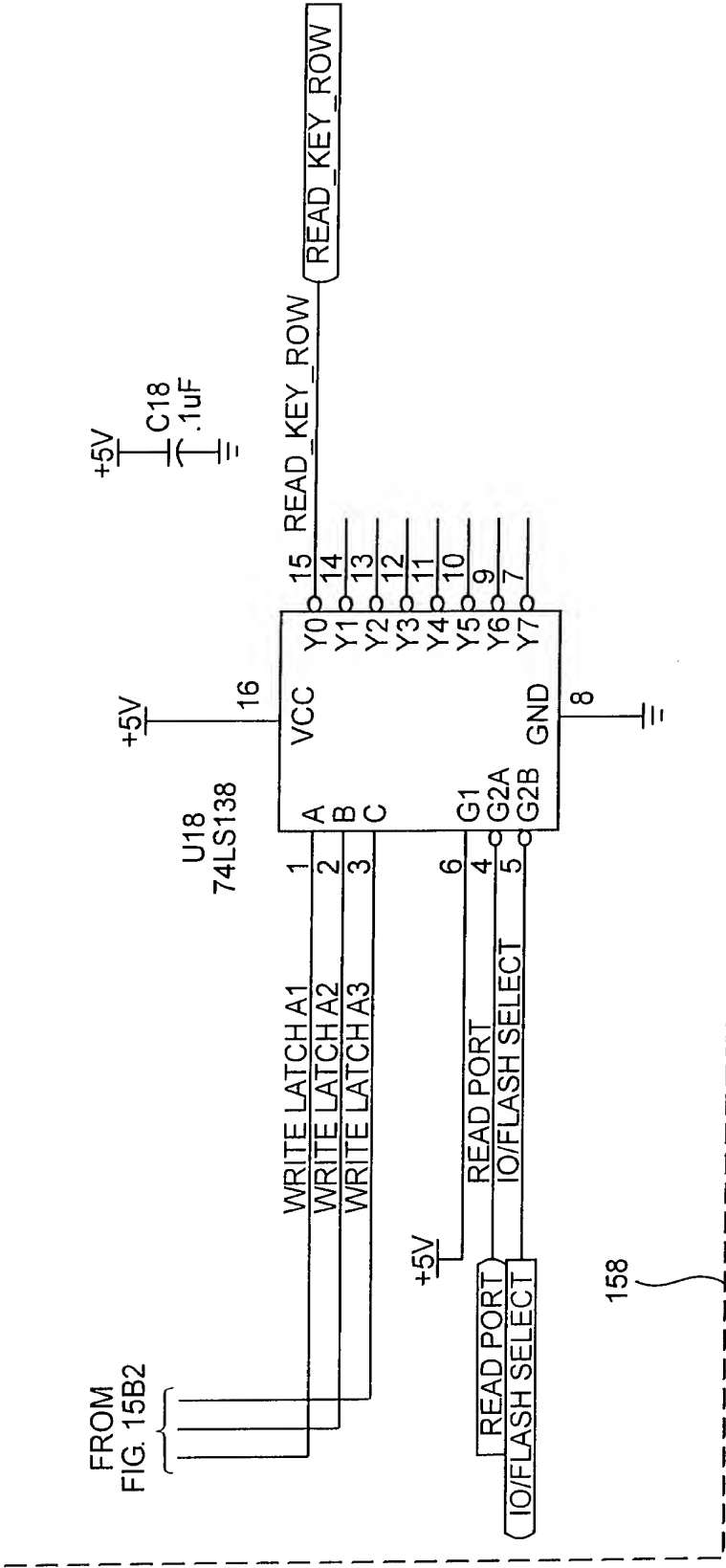


FIG. 15B2 CENTRAL DISPLAY BOARD



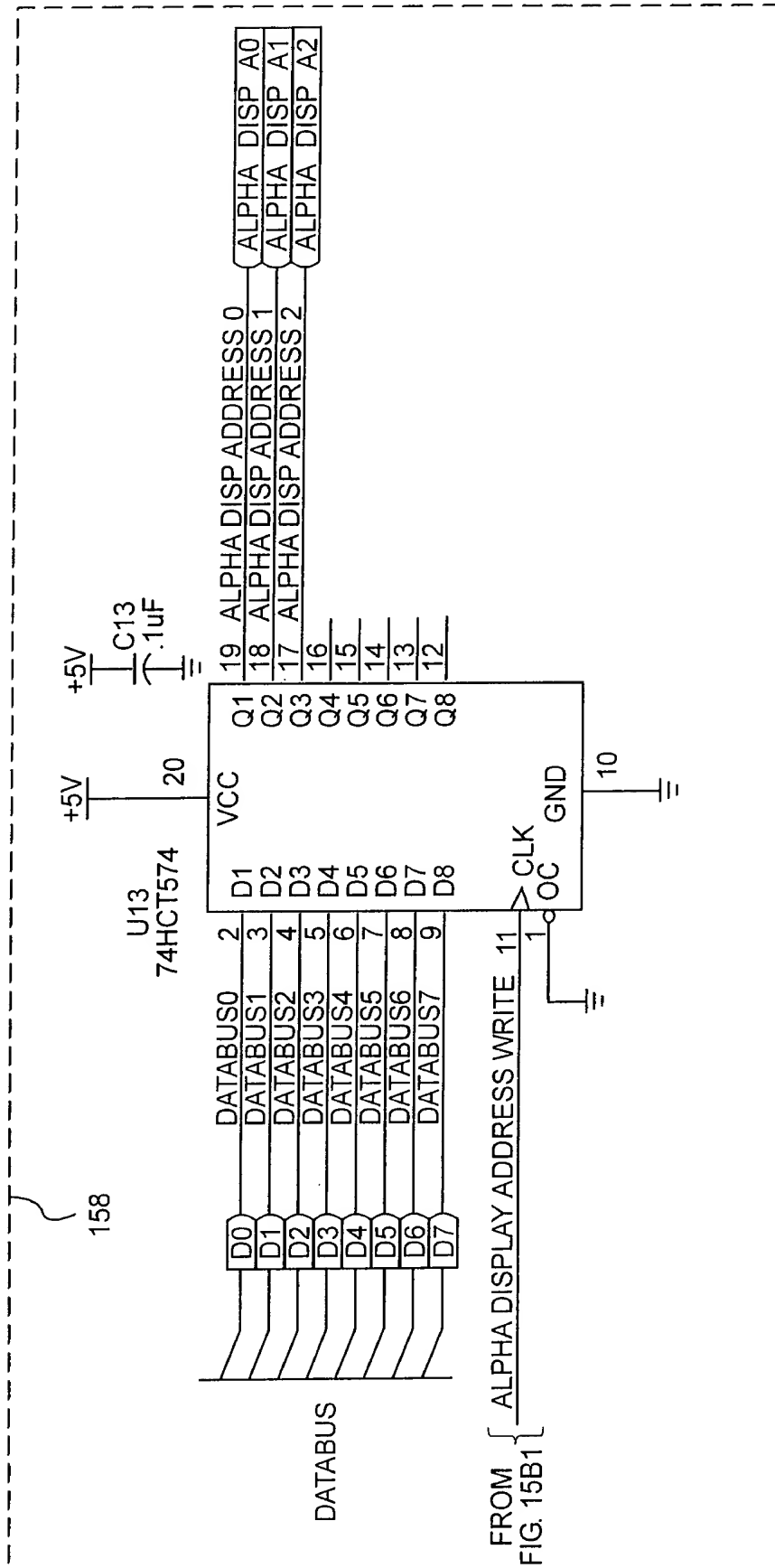
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FIG. 15B3 CENTRAL DISPLAY BOARD



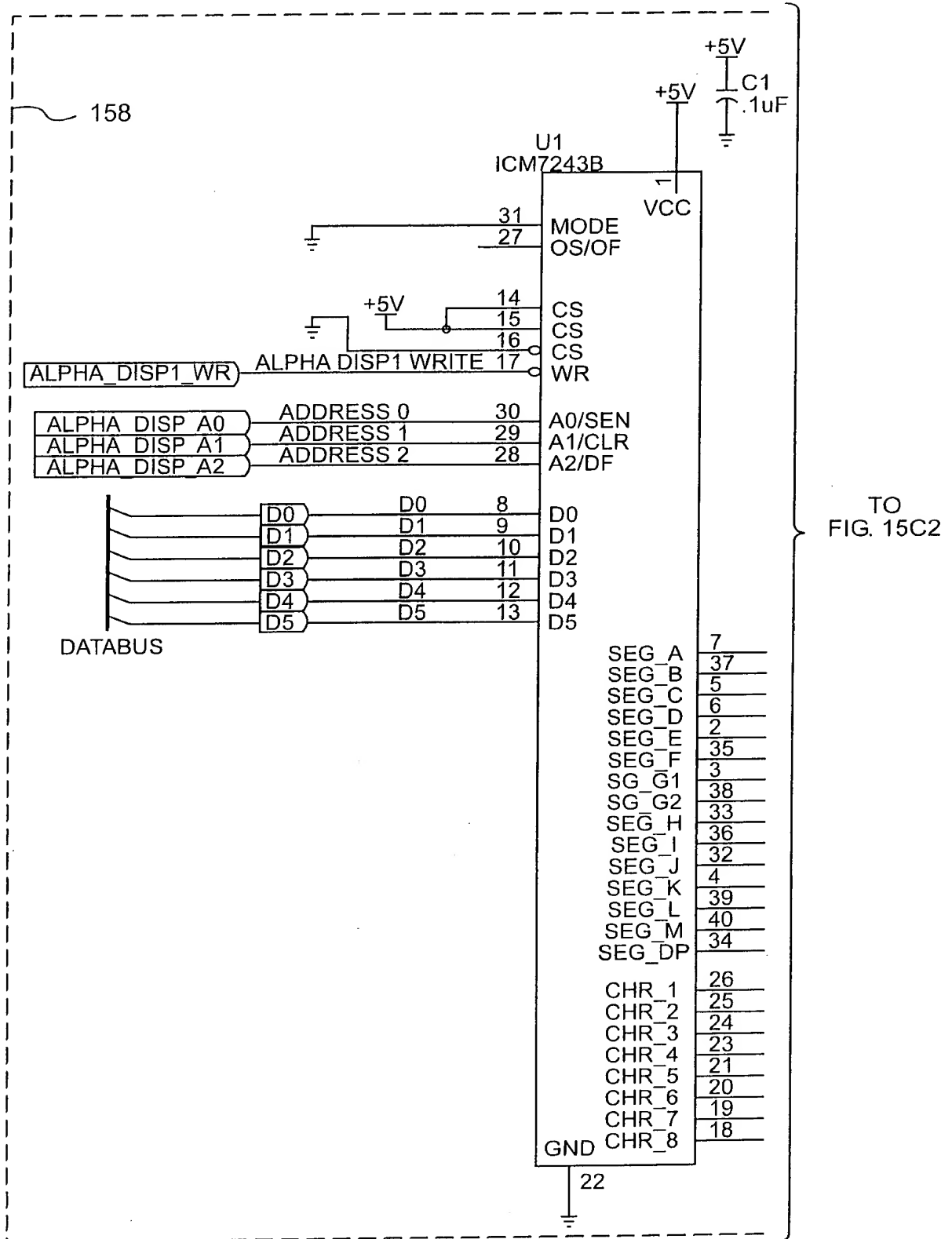
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FIG. 15B4 CENTRAL DISPLAY BOARD

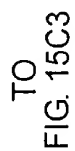


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FIG. 15C1 CENTRAL DISPLAY BOARD

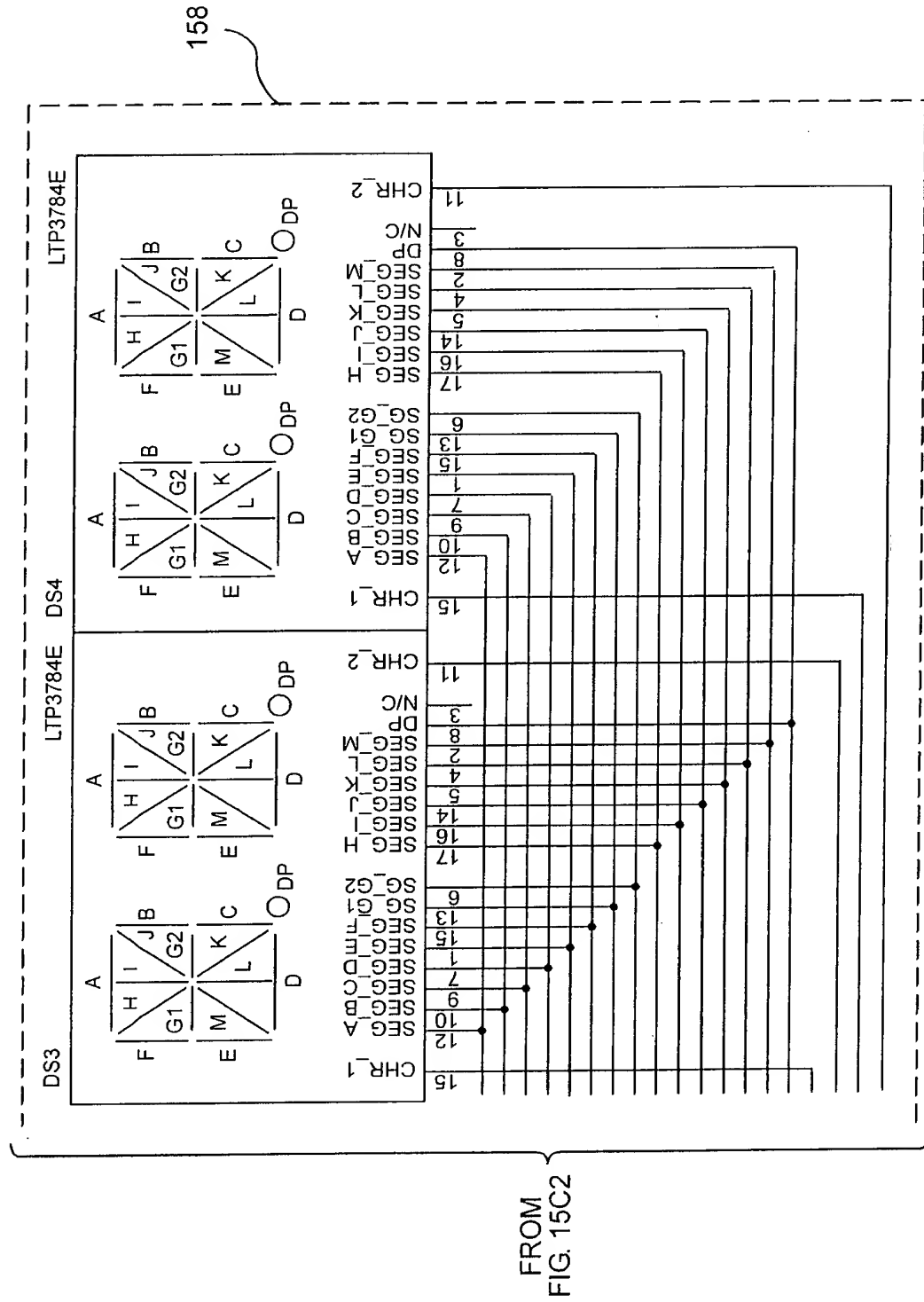


FROM
FIG. 15C1



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FIG. 15C3 CENTRAL DISPLAY BOARD



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FIG. 15D CENTRAL DISPLAY BOARD

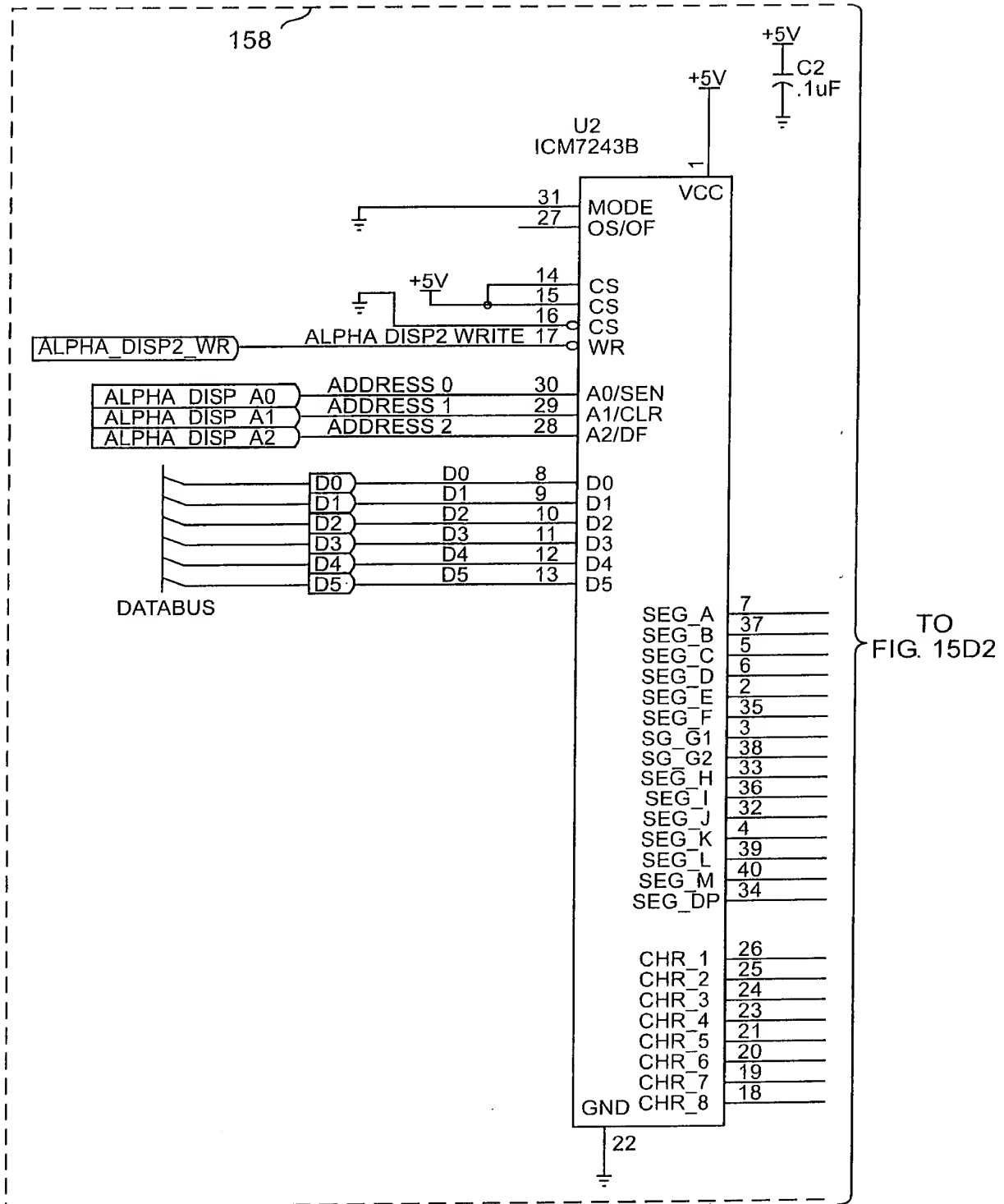
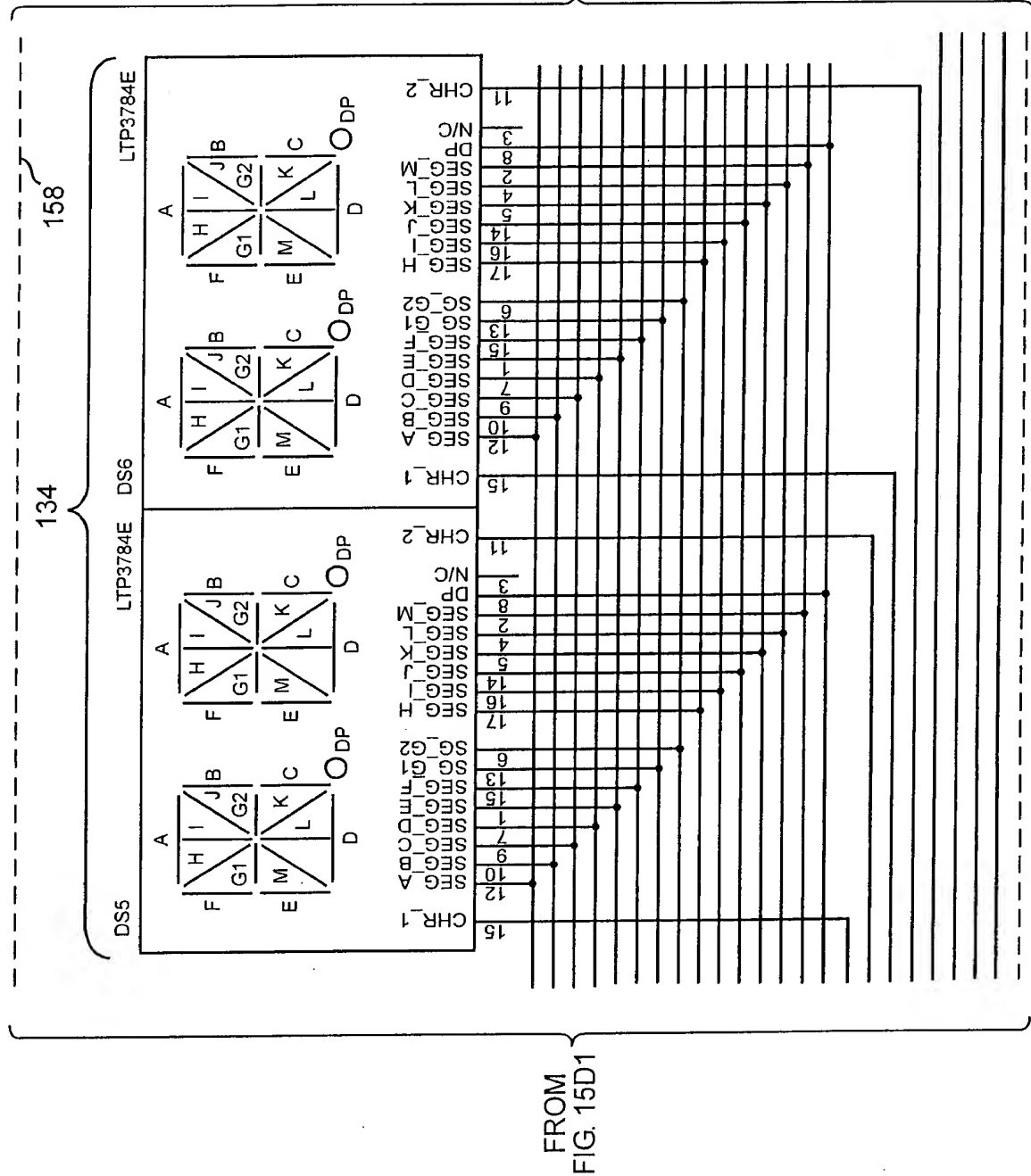
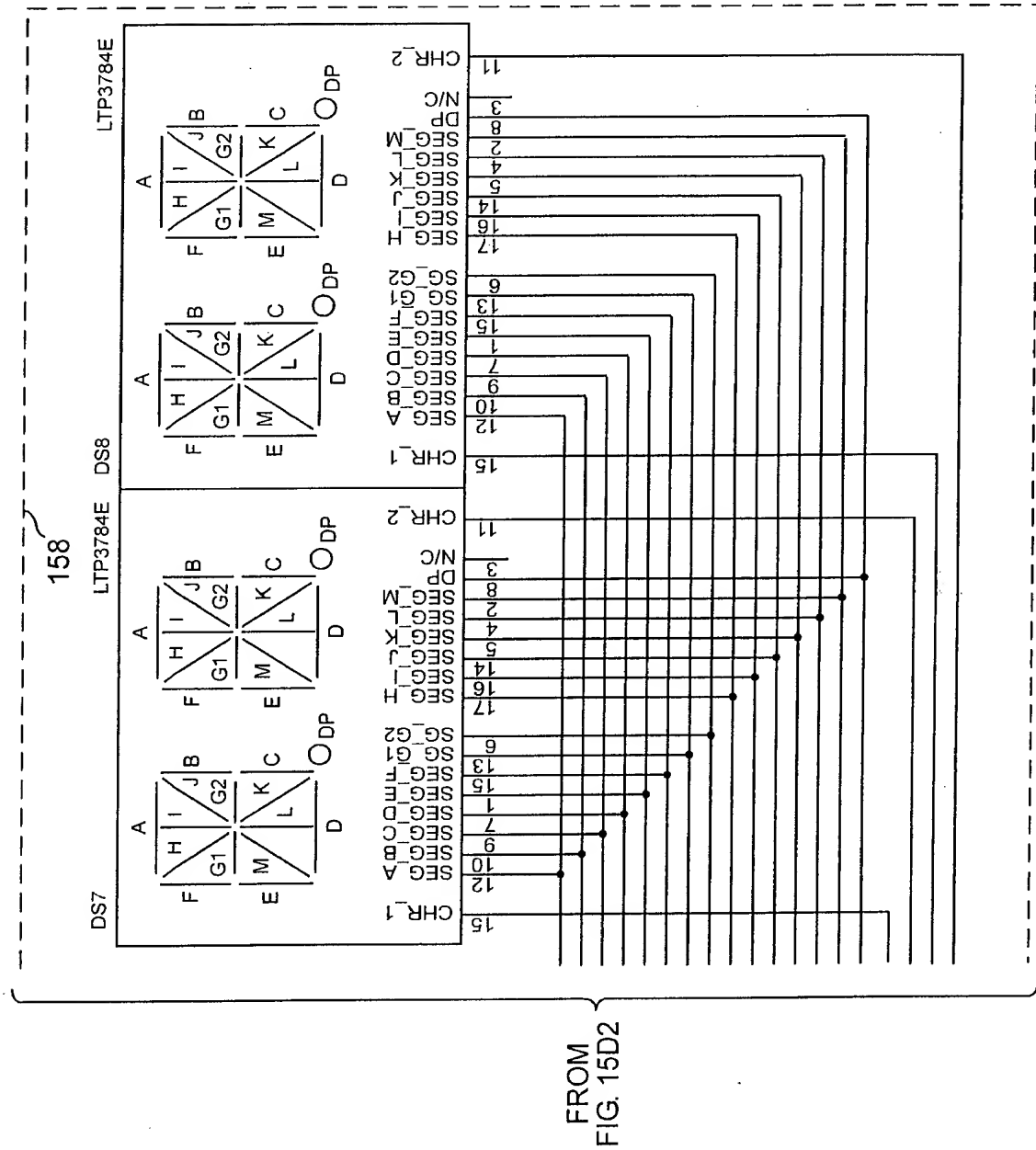


FIG. 15D2 CENTRAL DISPLAY BOARD



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FIG. 15D3 CENTRAL DISPLAY BOARD



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FIG. 15E1 CENTRAL DISPLAY BOARD

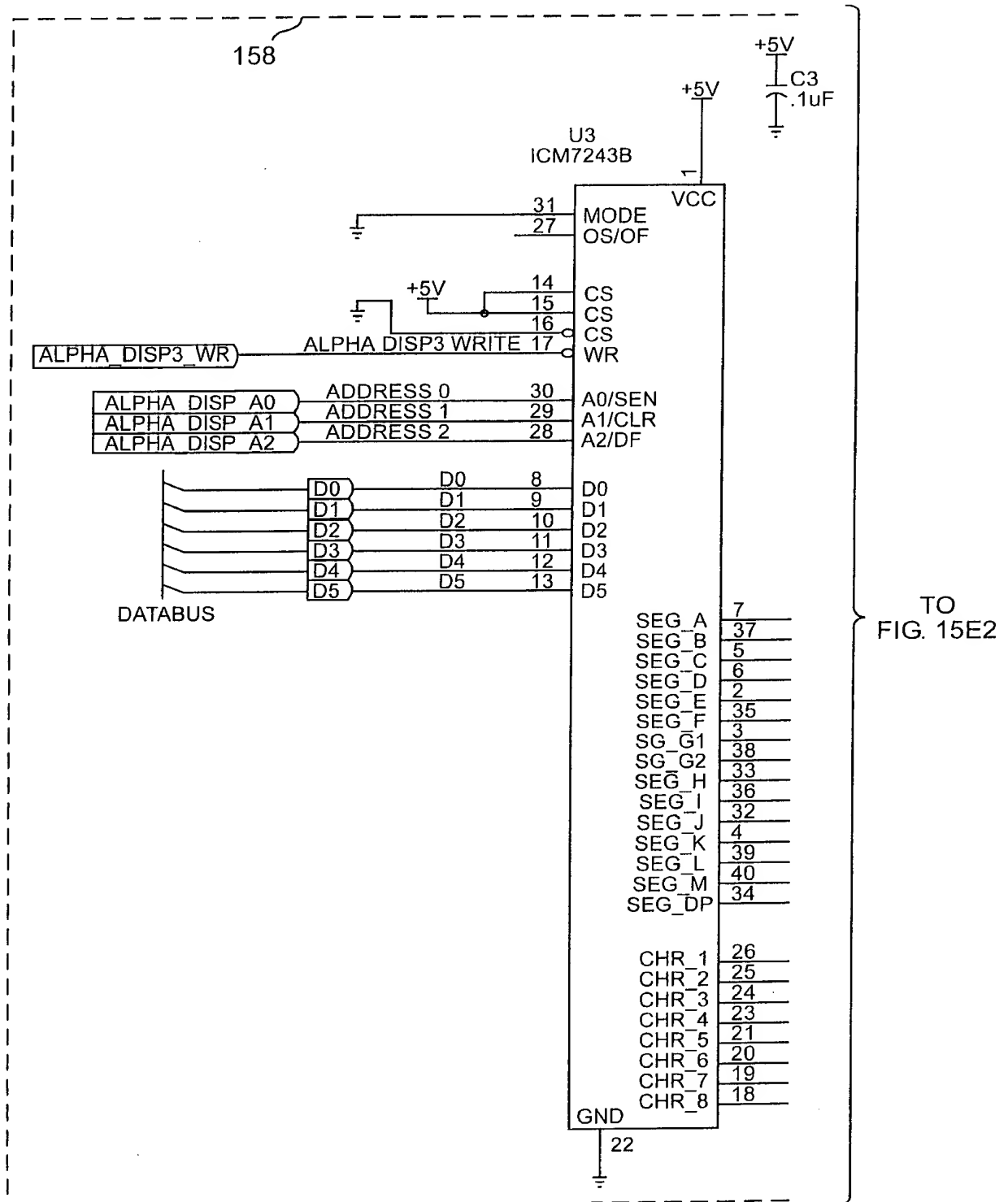
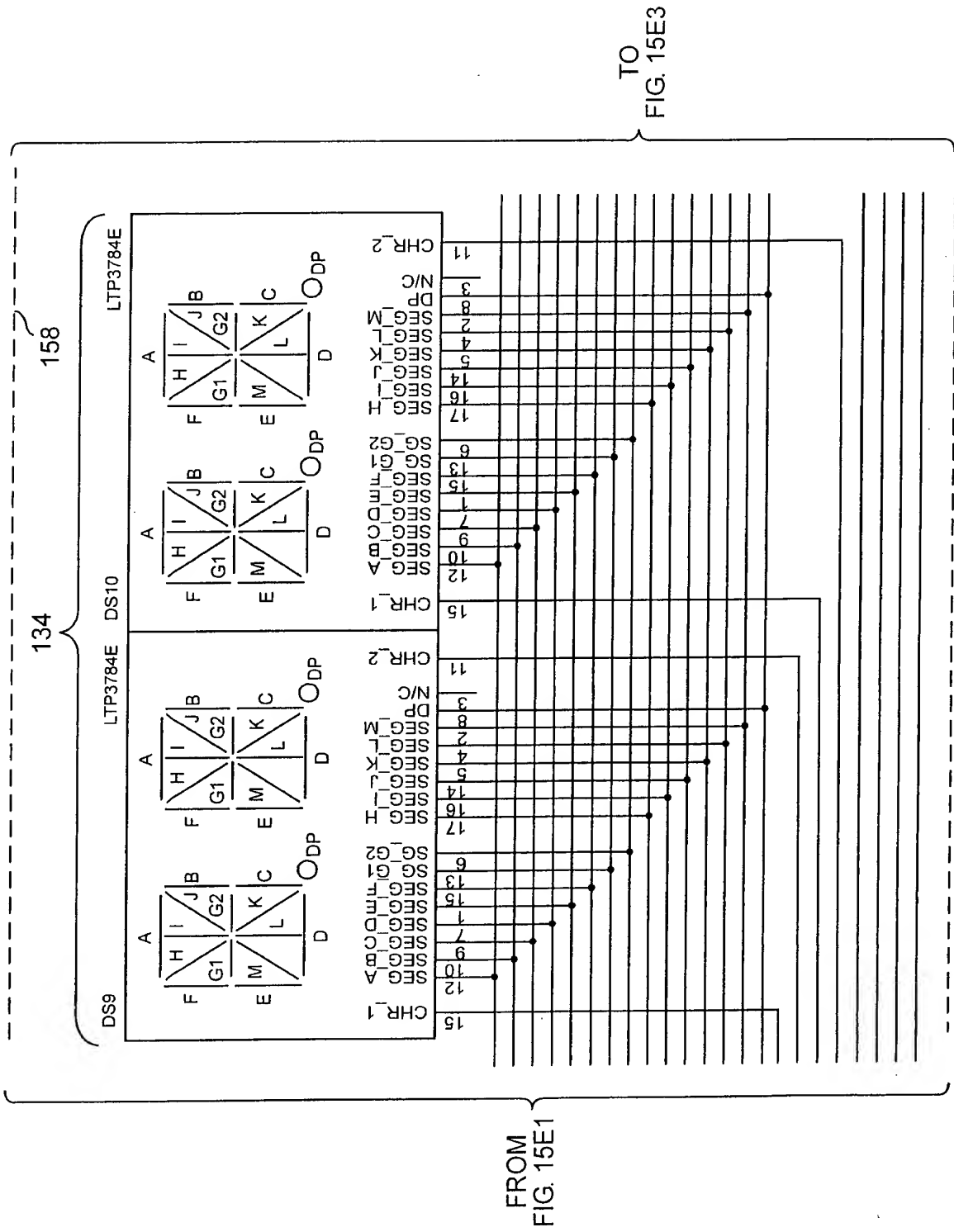
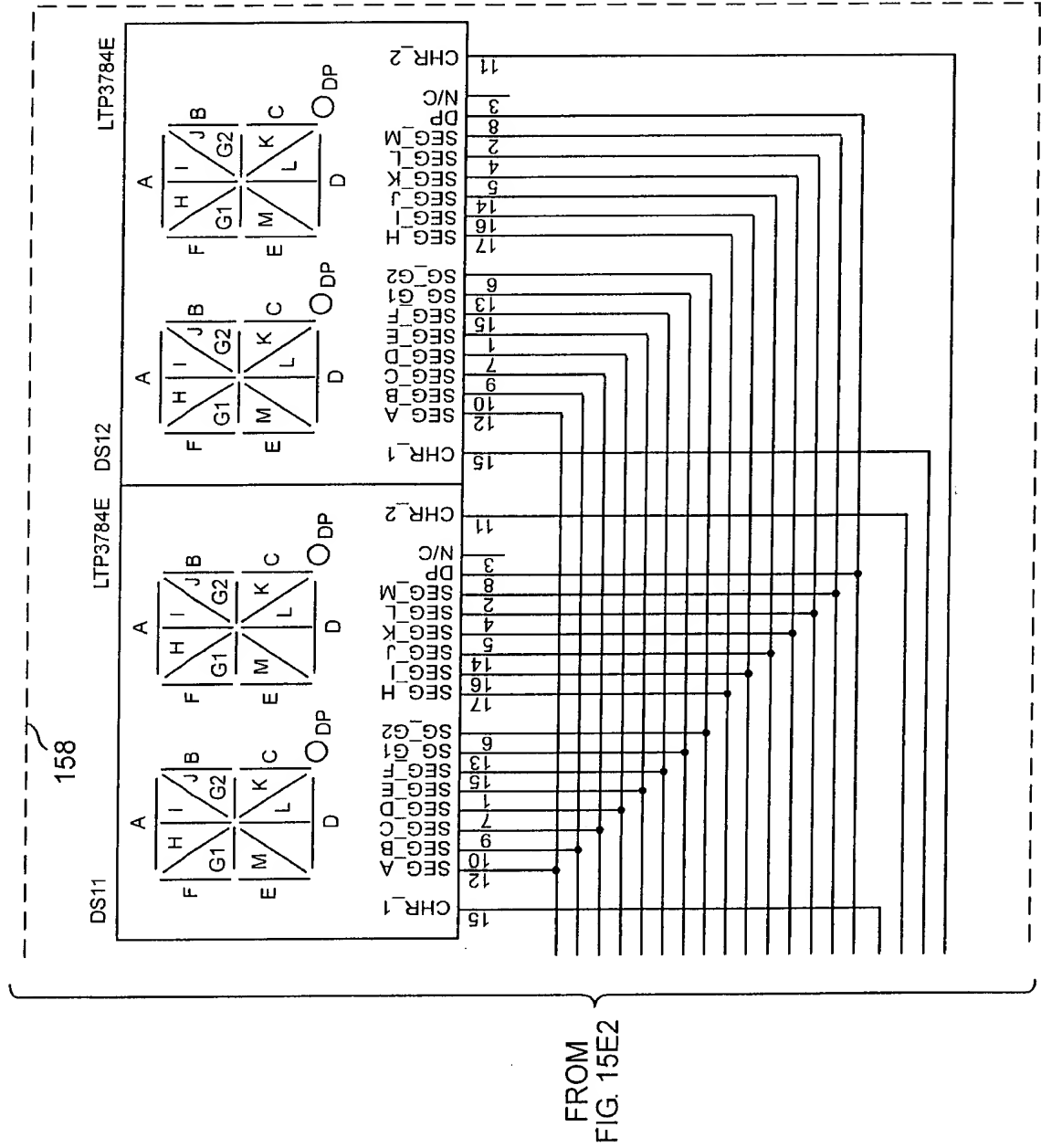


FIG. 15E2 CENTRAL DISPLAY BOARD



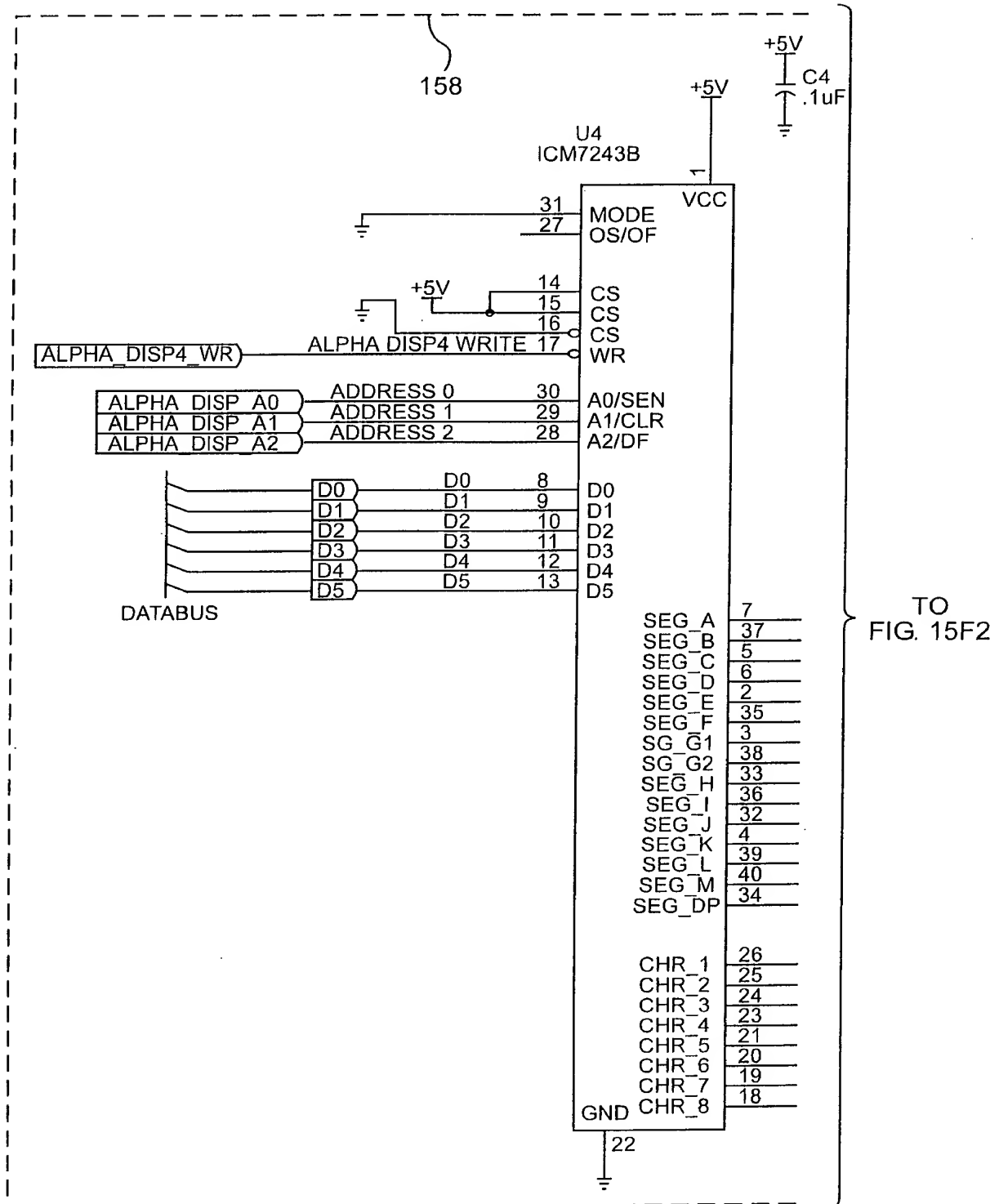
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FIG. 15E3 CENTRAL DISPLAY BOARD



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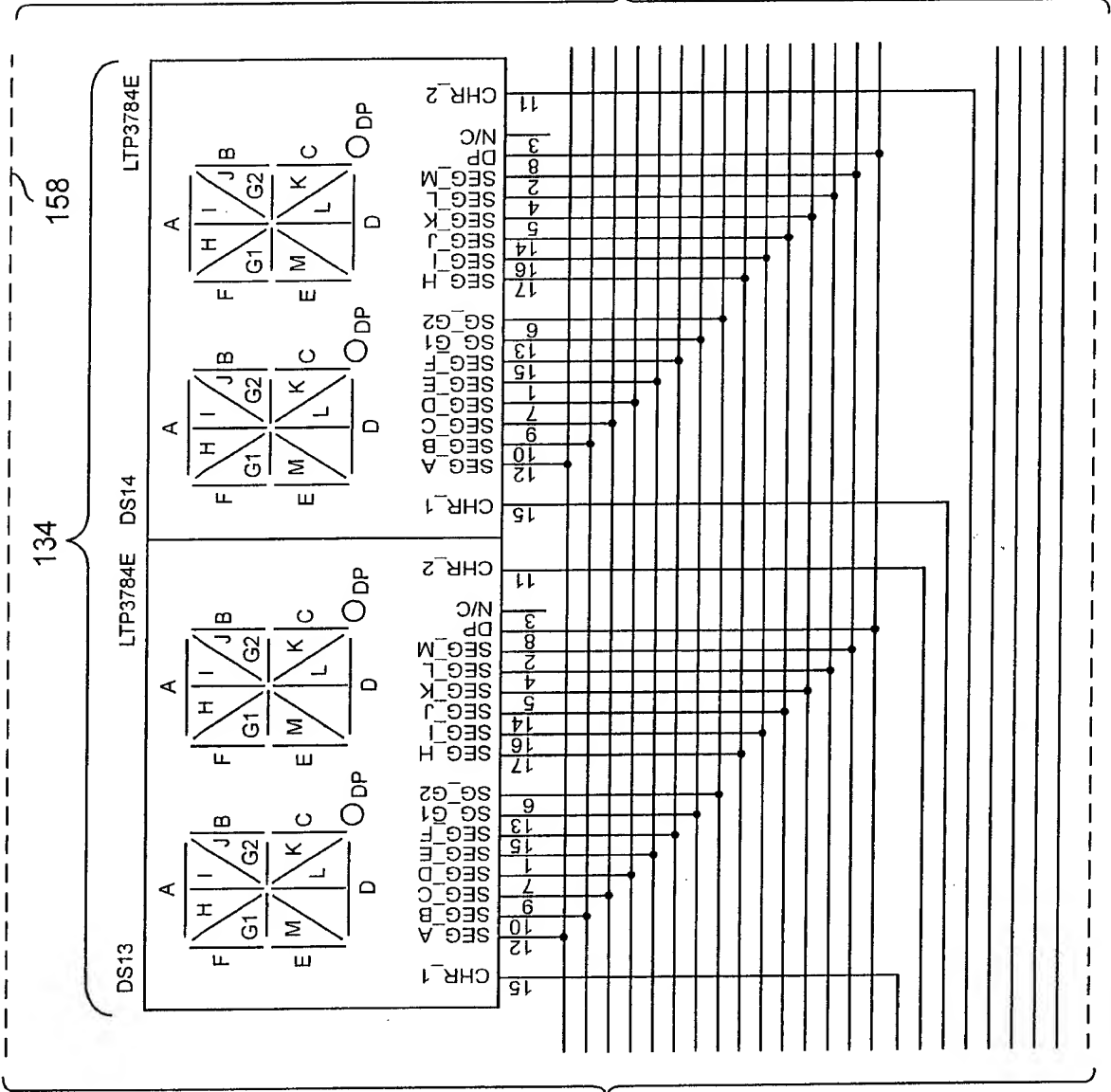
FIG. 15F1 CENTRAL DISPLAY BOARD



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TO
FIG. 15F3

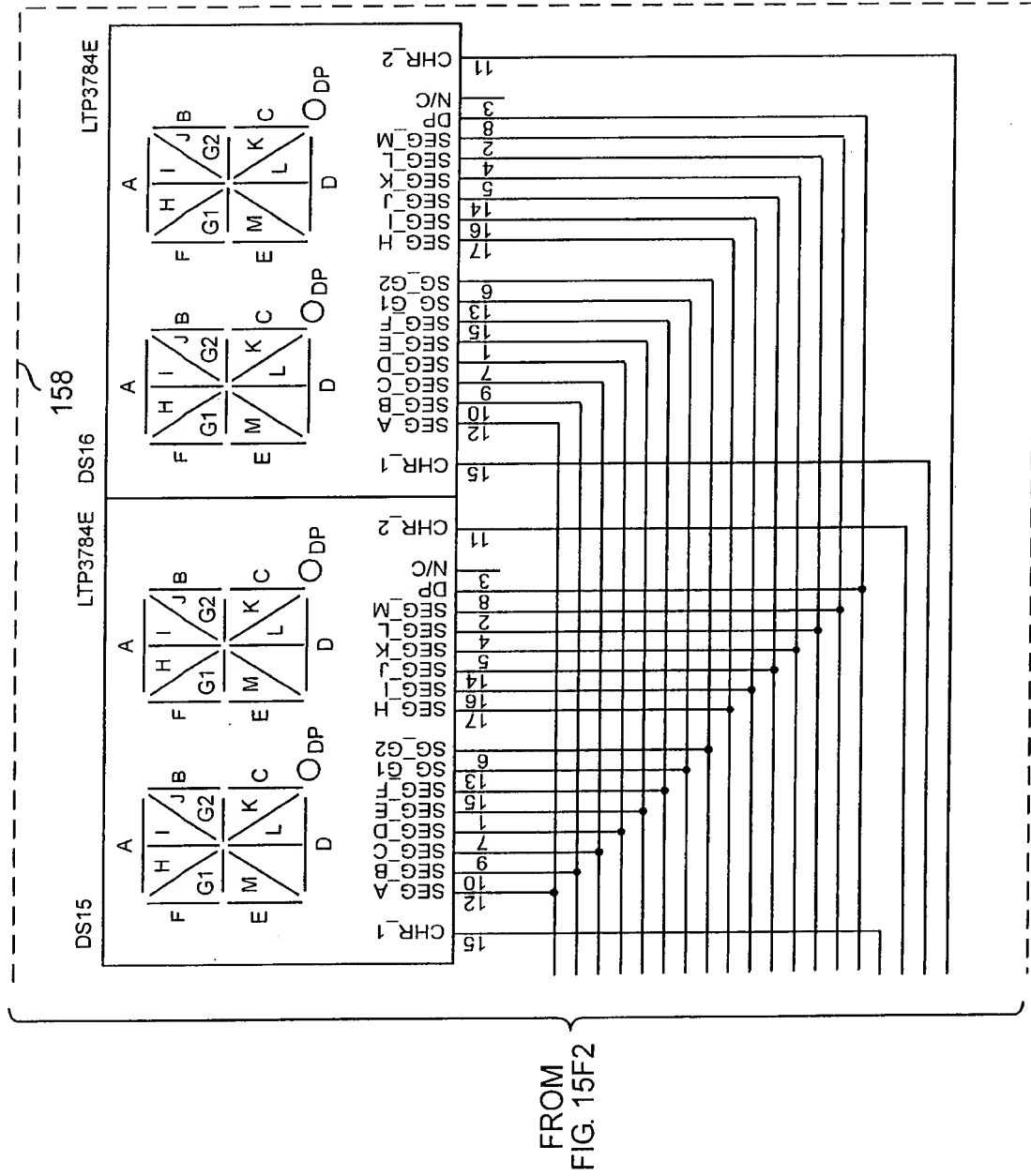
FIG. 15F2 CENTRAL DISPLAY BOARD



FROM
FIG. 15F1

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FIG. 15F3 CENTRAL DISPLAY BOARD



158

U5
ICM7243B

+5V
C5
.1uF

31 MODE
27 OS/OF

14 CS
15 CS
16 CS
17 WR

ALPHA_DISP5_WRITE

ALPHA_DISP_A0 ADDRESS 0 30 A0/SEN
ALPHA_DISP_A1 ADDRESS 1 29 A1/CLR
ALPHA_DISP_A2 ADDRESS 2 28 A2/DF

D0 8 D0
D1 9 D1
D2 10 D2
D3 11 D3
D4 12 D4
D5 13 D5

DATABUS

7 SEG_A
37 SEG_B
5 SEG_C
6 SEG_D
2 SEG_E
35 SEG_F
3 SG_G1
38 SG_G2
33 SEG_H
36 SEG_I
32 SEG_J
4 SEG_K
39 SEG_L
40 SEG_M
34 SEG_DP

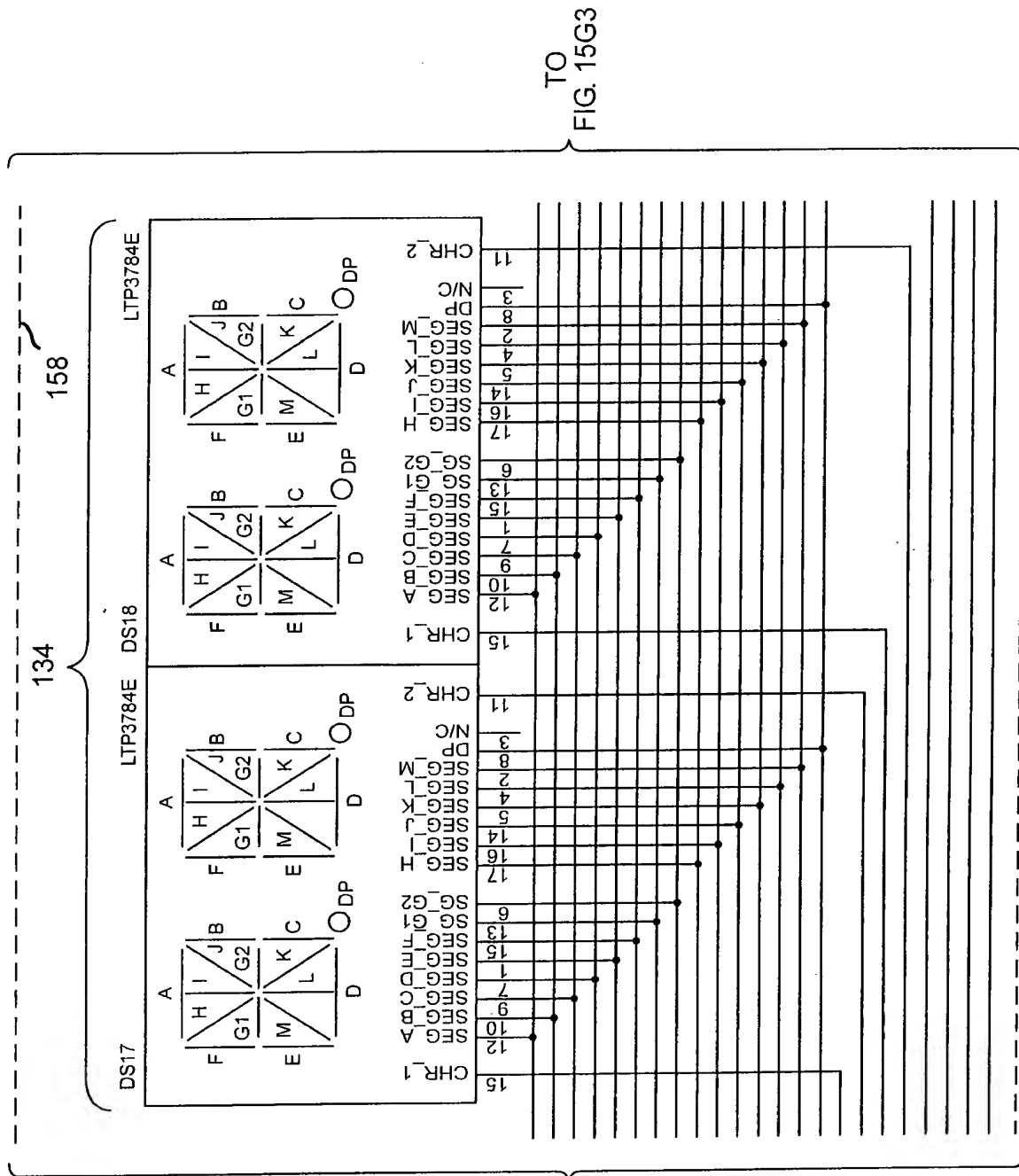
26 CHR_1
25 CHR_2
24 CHR_3
23 CHR_4
21 CHR_5
20 CHR_6
19 CHR_7
18 CHR_8

GND 22

TO
FIG. 15G2

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FIG. 15G2 CENTRAL DISPLAY BOARD



FROM
FIG. 15G2

FROM
FIG. 15G2

158

U6
ICM7243B

+5V

C6
.1uF

31
27
14
15
16
17

MODE
OS/OF

CS
CS
CS
WR

ALPHA_DISP6_WRITE

ADDRESS 0
ADDRESS 1
ADDRESS 2

ALPHA_DISP A0
ALPHA_DISP A1
ALPHA_DISP A2

D0
D1
D2
D3
D4
D5

DATABUS

SEG A
SEG_B
SEG_C
SEG_D
SEG_E
SEG_F
SG_G1
SG_G2
SEG_H
SEG_I
SEG_J
SEG_K
SEG_L
SEG_M
SEG_DP

CHR_1
CHR_2
CHR_3
CHR_4
CHR_5
CHR_6
CHR_7
CHR_8

GND

TO
FIG. 15H2

FROM
FIG. 15H1

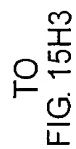
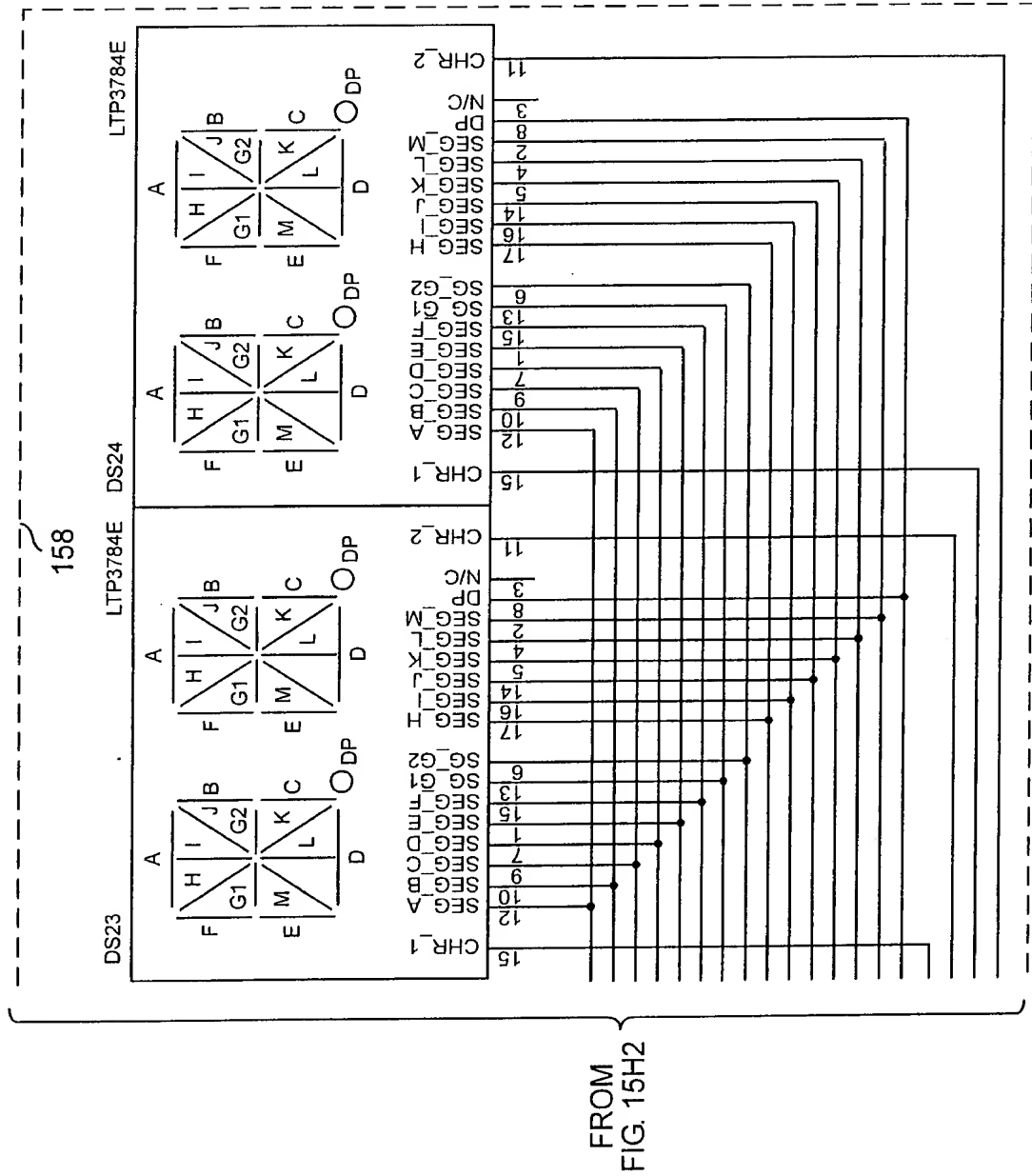
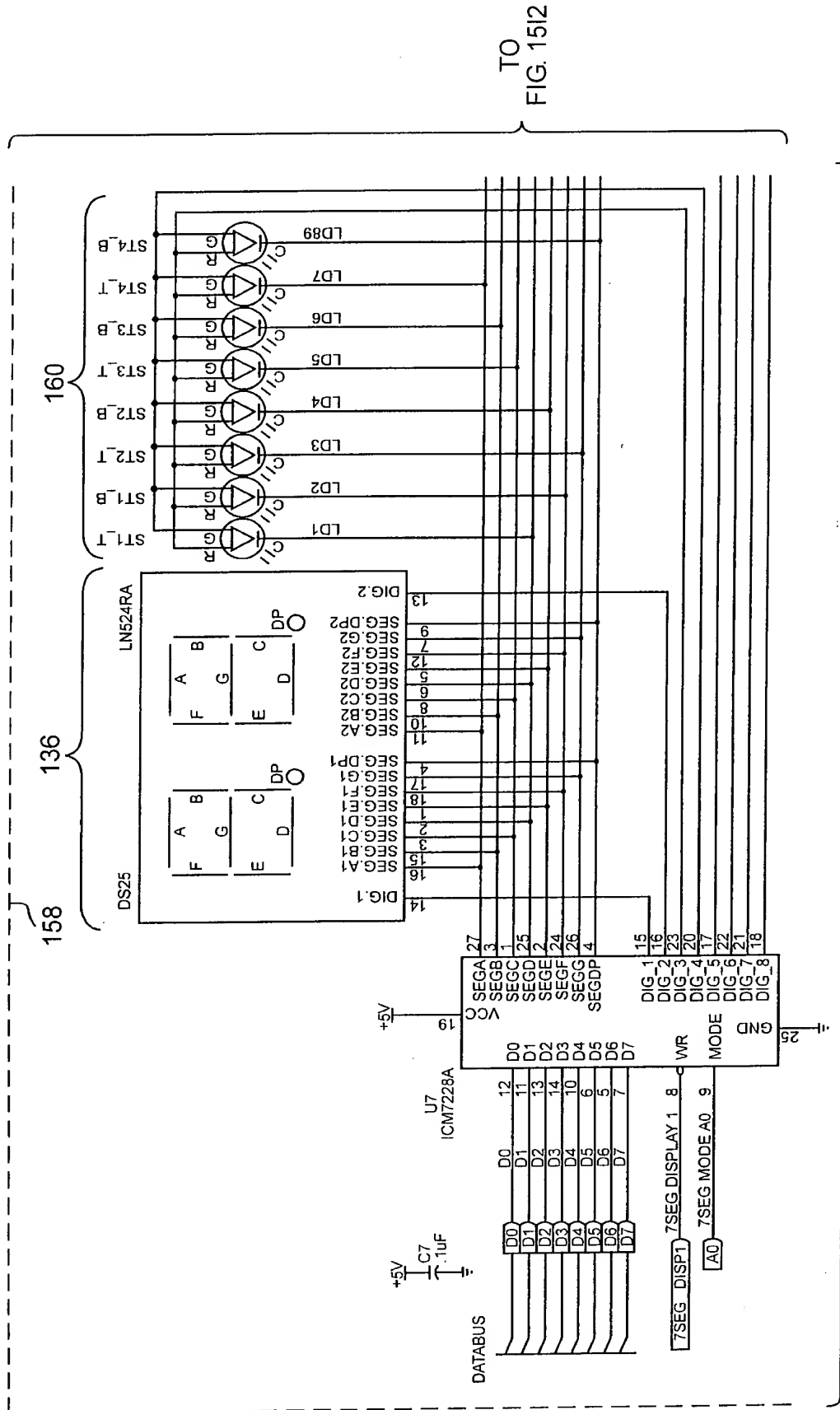


FIG. 15H3 CENTRAL DISPLAY BOARD



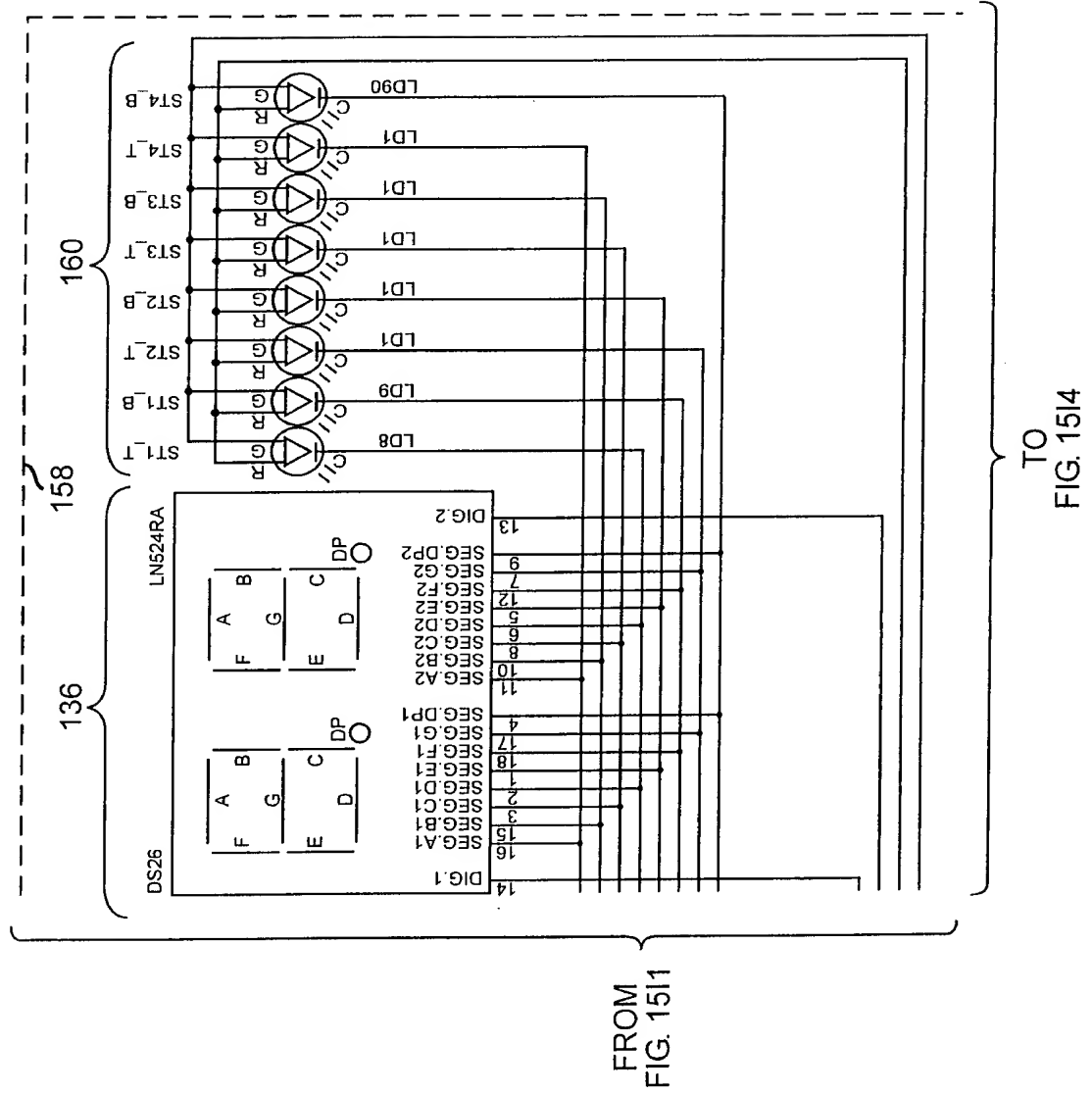
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FIG. 151 CENTRAL DISPLAY BOARD



TO
FIG. 1513

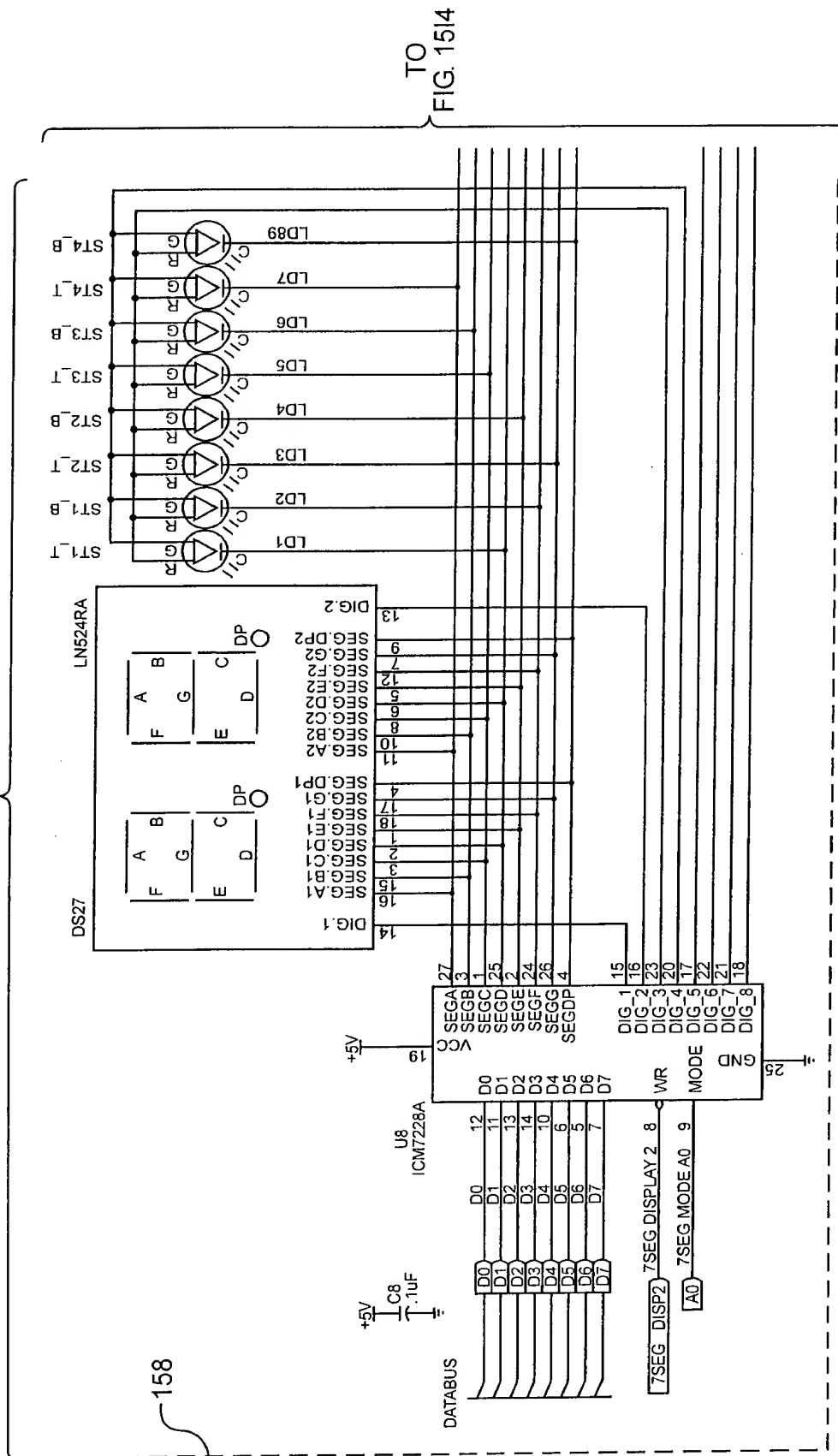
FIG. 1512 CENTRAL DISPLAY BOARD



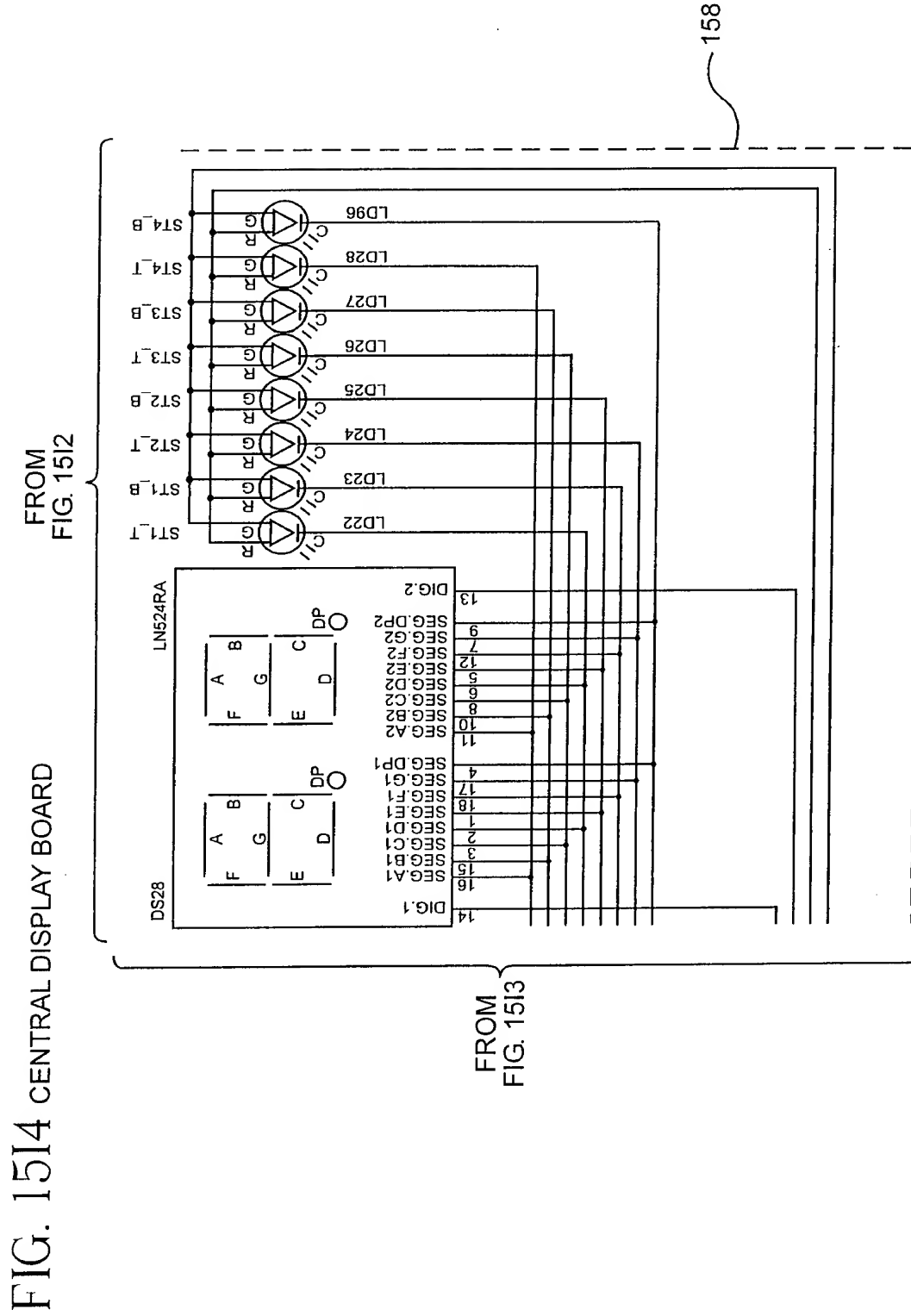
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FIG. 15I3 CENTRAL DISPLAY BOARD

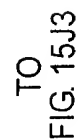
FROM
FIG. 15I1



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TO
FIG. 15J2



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FIG. 15J2 CENTRAL DISPLAY BOARD

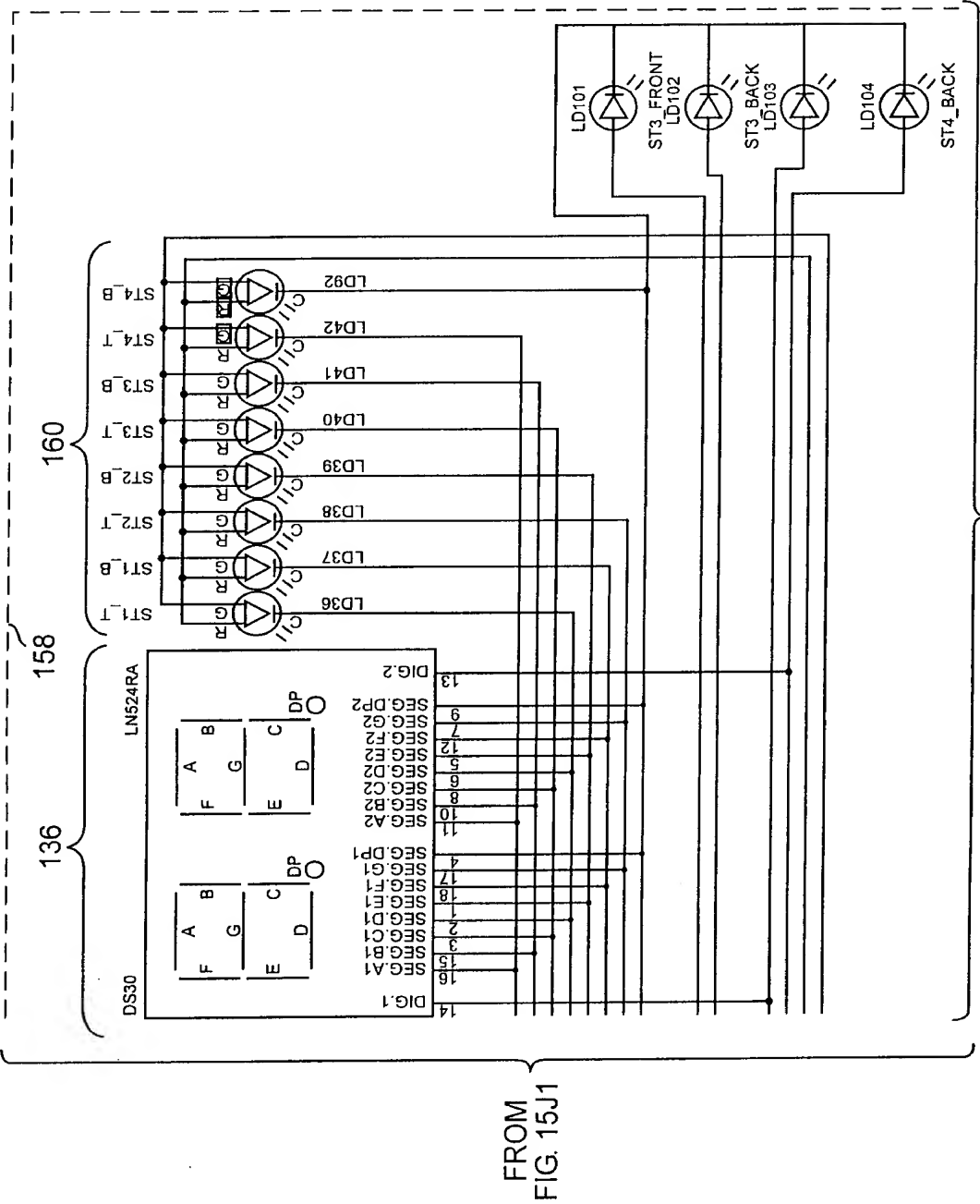
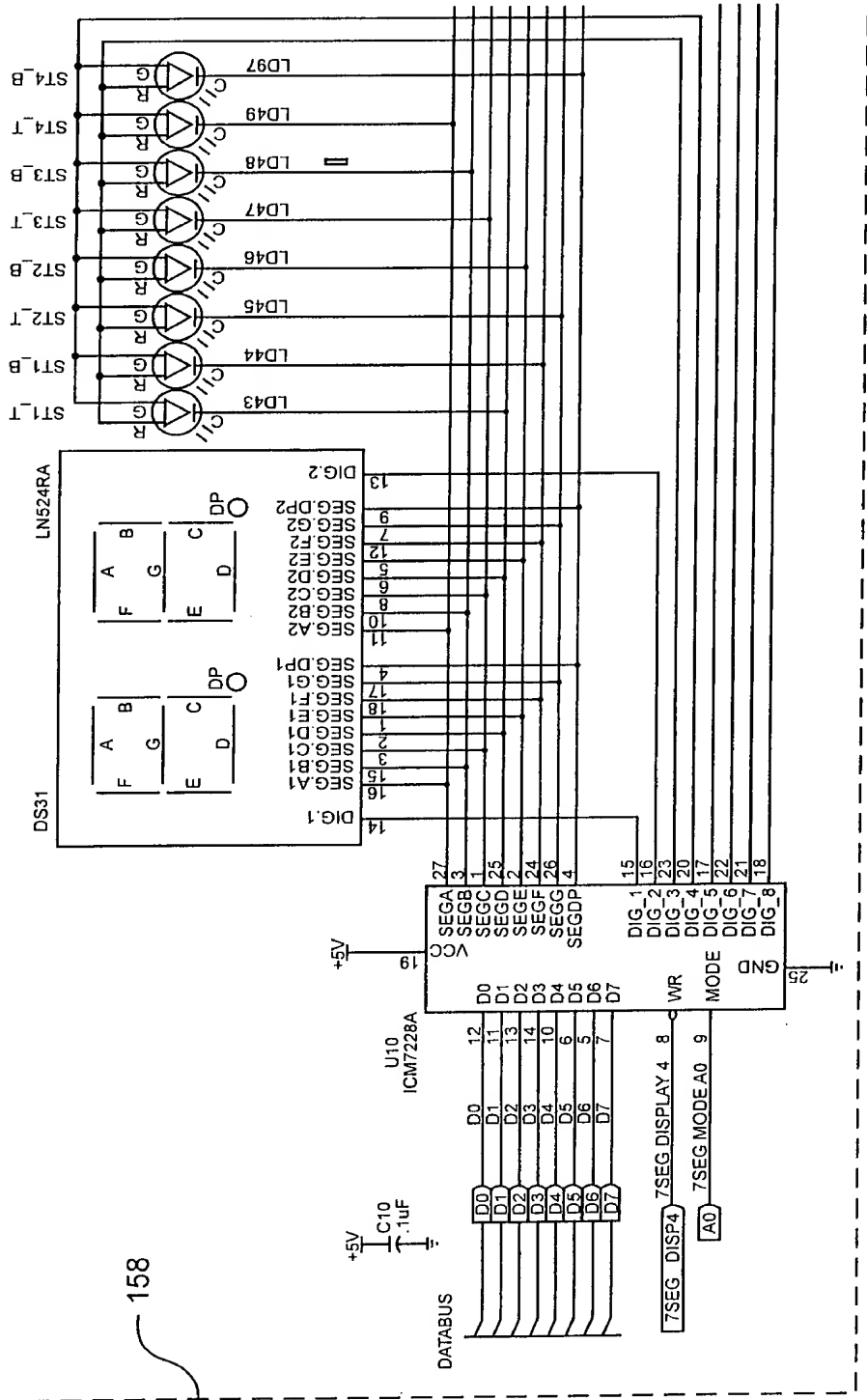


FIG. 15J3 CENTRAL DISPLAY BOARD

FROM
FIG. 15J1

TO
FIG. 15J4

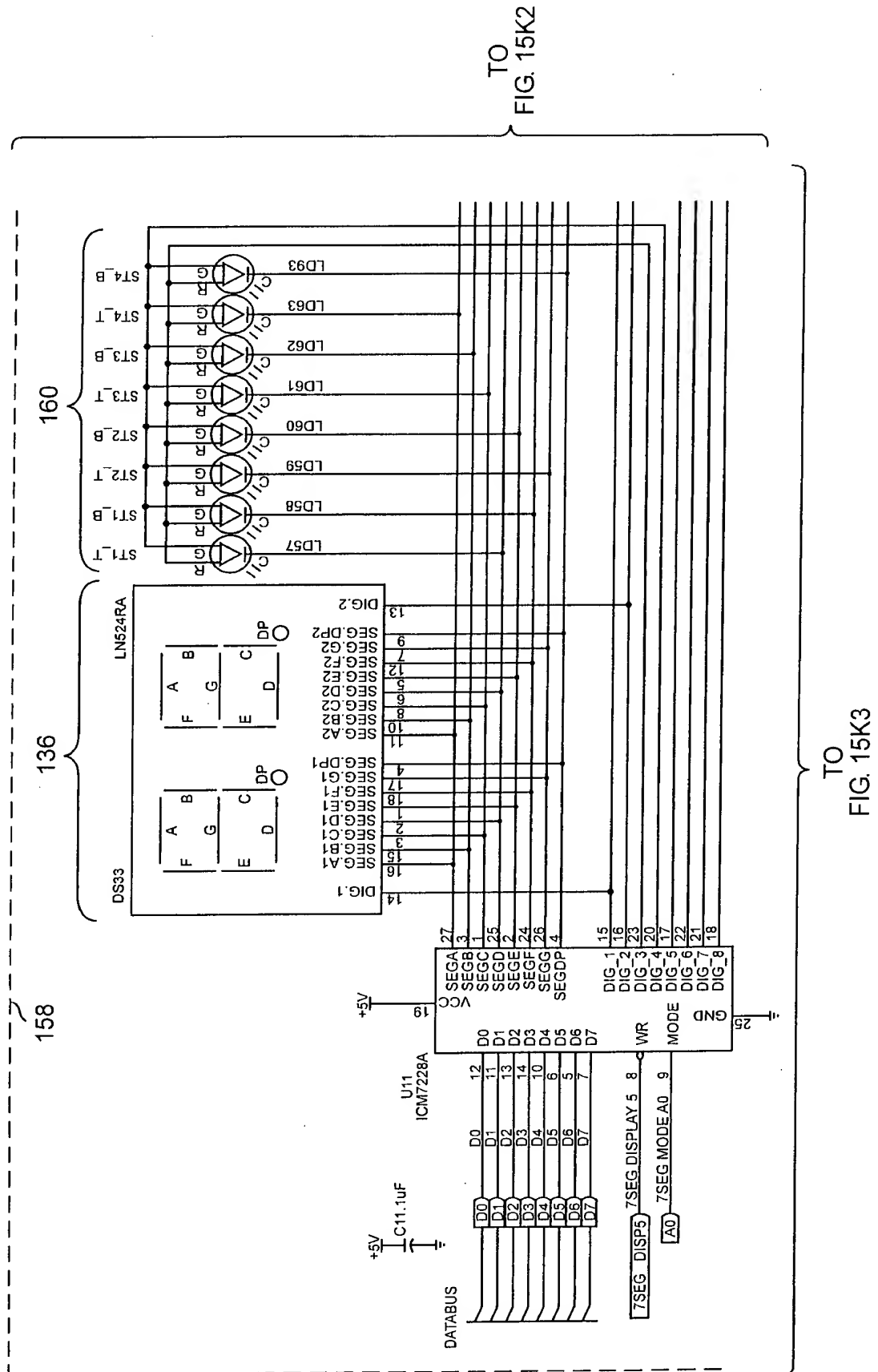


FROM
FIG. 15J2



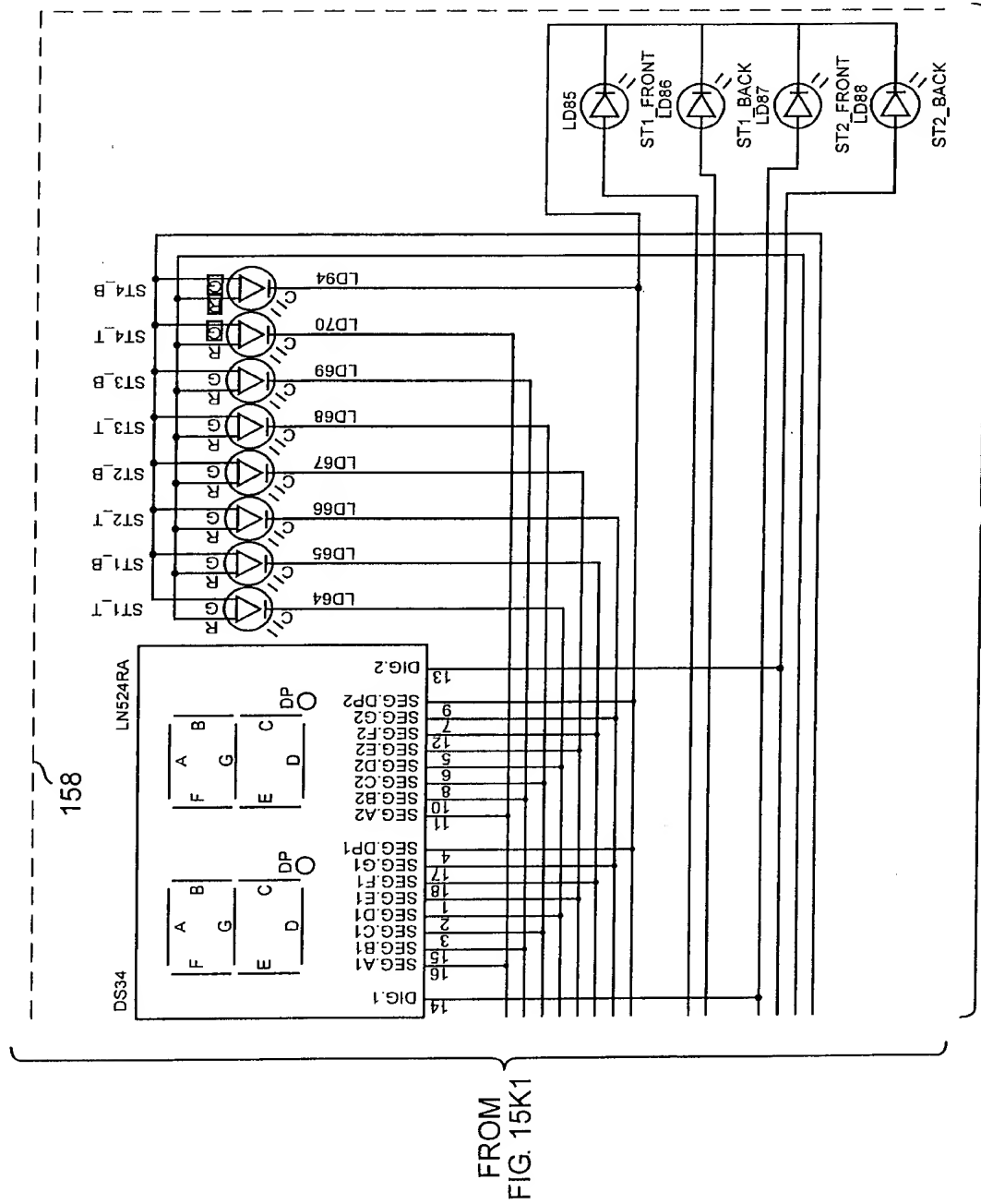
FROM
FIG. 15J3

FIG. 15K1 CENTRAL DISPLAY BOARD



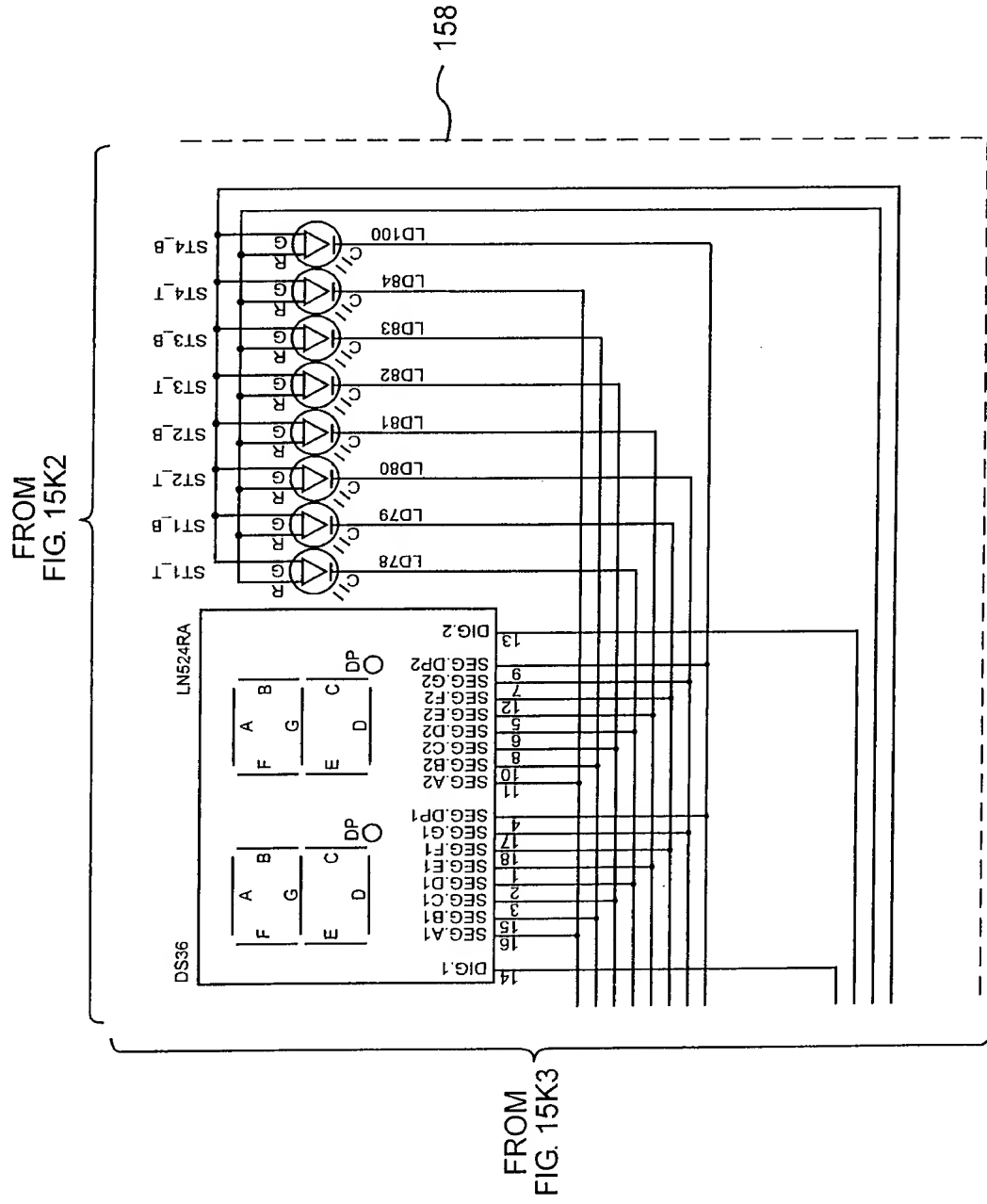
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FIG. 15K2 CENTRAL DISPLAY BOARD



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FIG. 15K4 CENTRAL DISPLAY BOARD



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FIG. 15L CENTRAL DISPLAY BOARD

